A NOVEL 3 VOLTS-ONLY, SMALL SECTOR ERASE, HIGH DENSITY FLASH E²PROM

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Abstract A split gate Flash E²PROM memory cell with Fowler-Nordhiem tunneling erase, and high efficiency hot electron programming is presented (1). Gate current measurements show that one out of every 300 channel electron is injected into the gate under worst case programming conditions (2). The greater efficiency of cell allows the use of small on-chip multipliers for single 3v Vcc operation. High cell reliability is achieved through low floating gate oxide field (oxide reliability) and small programming current (contact reliability). It is shown that the cell is immune to read and write disturb conditions.

Introduction High density Flash E²PROM suitable for mass storage applications require small power consumption, fast write and read as well as adaptability to low voltage operations. The technology presented here, is based on dual poly silicon, and single metal interconnect. The major process sequence and resulting silicon are depicted in Figure (1). The cell utilizes a source side hot electron injection scheme for write and an interpoly FN tunneling mechanism for sector erase (2). The cell operation is described in figure (2).

The floating gate is strongly coupled to high voltage diffusion node. The word line acts as the select gate and also as the erase element. Since the bit line is never subjected to high voltage, the isolation size can be reduced to minimum geometry. The resulting cell is very compact. Due to split gate approach there is no over-erase or over-program problem which in turn simplifies the peripheral circuitry thus resulting in high array efficiency.

Cell Operation As compared to the traditional FLOTOX technology, in which injection efficiency is low, this cell achieves very high efficiency. During programming operation the lateral electric field is very strong in region between the two gates. The vertical field across the floating gate oxide is always favorable for collecting hot electrons. Figures (3) show simulated fields (lateral and vertical) during write operation.

Measurement on a cell with accessible floating gate shows that a ~2volts swing on the floating gate is required to change the "0" to "1" state (figure 4). Greater than 80% of the high voltage (V_{pp}) couples to the floating gate (CR_s) leaving 20% coupling from the select gate(V_{wl}) to floating gate (CR_g). During programming we estimate the floating gate voltage (Vfg) to be,

$$V_{fg} = V_{fg}^{Q} + CR_g * V_{wl} + CR_s * V_{pp}. \quad (1)$$

Where V_{fg}^{Q} is the voltage resulting from charge. Substituting nominal programming conditions (Vpp=11, Vwl=2, V_{fg}^{Q} =2.7~0.7) into above equation results in V_{fg}=11.9v~9.9v from initial to final programming stage respectively.

Using the worst case scenario, 3 out of 1000 channel electrons are collected by the gate (Figure 5). The programming time of a typical cell is <15uSec. Figure (6) shows the impact of Vpp and oxide charge on writing efficiency. Higher Vpp increases the channel field and thus results in more efficient write. The charge trapping during write operation degrades the write efficiency slowly (i.e. <3X in 100K write cycles), allowing continued fast programming.

The erase operation is achieved by FN tunneling from the floating gate to the select gate which spans one row. The tunneling oxide process is designed to produce a field enhancement corner along the edges of the floating gate (figure 1). The low coupling ratio between the select and floating gates allow build up of a significant voltage across the tunnel element. Only a fraction of the available high voltage is required to erase the cell in early life. Erase efficiency of the cell is excellent due to the field enhancing feature of the tunnel element.

Disturb The read and erase conditions are similar except for word-line voltage level. Therefore, continuous read should be guaranteed without disturb. Figures (7) shows read disturb data and projected behavior for operating bias condition. A FN-tunneling fit predicts a very long read disturb immunity exceeding hundreds of years.

The write disturb can be caused by tunnel disturb (TD) for unselected bit-line, or punch through (PT) for unselected word-line. The write disturb data is summarized in figure (8) . Since TD is insensitive to temperature, the increase in disturb at elevated temperature is mainly due to PT.

Due to the fact that tunnel element has a field enhancing feature in "forward" (or erase) direction a large rectification ratio for reverse/forward tunnel voltage is achieved. This diode-like behavior is very effective in suppressing the TD.

In PT mode the cells experience Vpp while write is inhibited by virtue of high bit line voltage (Vcc) or grounded word-line. Both schemes are very effective in suppressing the PT mode.

References

[1]: H. Dill and T. Toombs, "A new MNOS charge storage effect," Solid-State Electronics, vol.12, pp.981-987, 1969.

[2]: M. Kamiya, Y. Kojima, Y. Kato, K. Tanaka, and Y. Hayashi "EPROM Cell with high gate injection efficiency," IEDM tech. Dig., 1982, p741.

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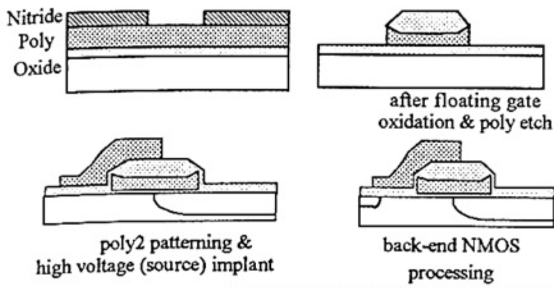

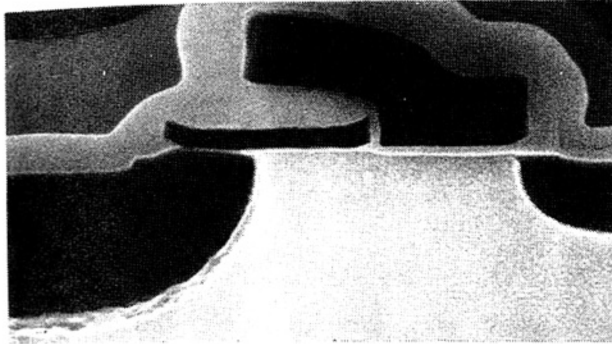

Fig.1: Sequence of memory cell processing & SEM cross section (30KX).

Operation	Word Line	Source Line	Bit Line
Erase	14V	0V	0V
Program	Vt	11V	0V Data "0" Vcc Data "1"
Read	Vcc	0V	2V

Fig 2: Memory cell operation table.

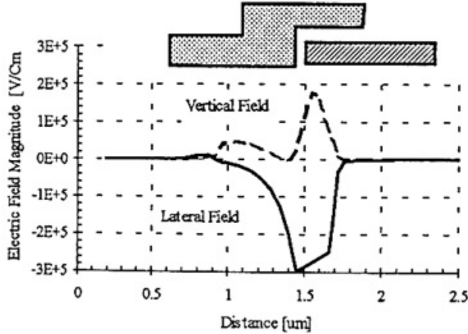

Fig 3: Simulated lateral and vertical fields during programming. Vpp=12 and CRg=80%.

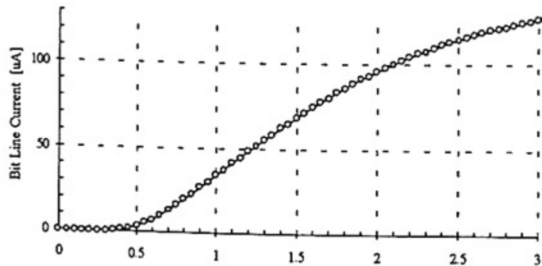

Fig 4: Non-floating gate cell IV characteristics. Normal read condition are used for word-line and bit line biasing.

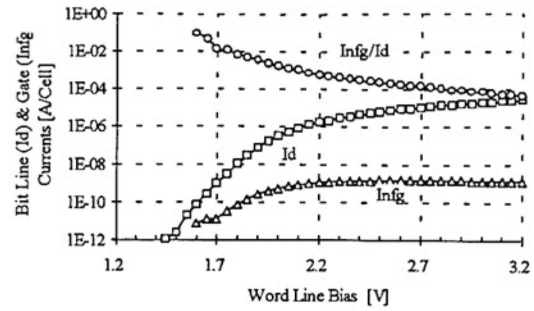

Fig. 5: Hot electron injection efficiency. Vpp=11v, Vnfg=9.5v. With 2v word line bias, the efficiency is ~3/1000.

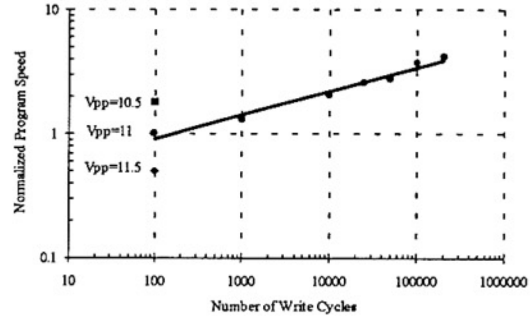

Fig. 6: Hot electron programming efficiency and programming time degredation with repeated cycling.

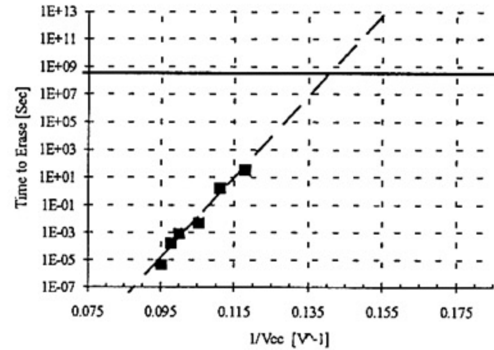

Fig. 7: FN tunneling erase efficiency and read disturb characteristics of the cell. The fitted line predicts >>10year disturb immunity.

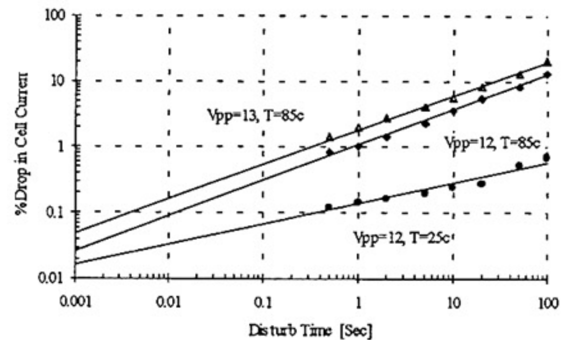

Fig. 8: Write disturb characteristics of the cell. A projection for a typical disturb period shows negligible impact.