Observations of Single Electron Trapping/Detrapping Events in Tunnel Oxide of SuperFlash® Memory Cell

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Abstract—Erase instabilities and erase performance degradation due to single-electron trapping events in tunnel oxide of SST split-gate SuperFlash® memory cells have been detected and analyzed for the first time. Whereas the instabilities of erase characteristics in stacked-gate flash memories ("erratic erase") are attributed to hole traping/detrapping associated with anode hole injection, SuperFlash® cell does not show any hole-related processes in tunnel oxide. A different behavior of SuperFlash® cell compared to conventional stacked-gate cell during erase operation due to different cell structures has been analyzed.

***Index Terms*—EPROM, tunneling, charge carrier processes, charge injection, hot carriers.**

I. Introduction

Electron trapping in charge-transfer dielectrics is known to be a limiting factor of program/erase cycling endurance of non-volatile floating-gate memories. In flash memory cells, which use channel hot-electron injection for programming and Fowler-Nordheim tunneling for erase, electron trapping in the tunnel oxide reduces electric field during erase operations, which results in gradual degradation of erase characteristics and closure of memory cell threshold window [1]. The understanding of charge trapping/detrapping kinetics is therefore needed for development of optimized program/erase schemes and memory cell design.

Another problem, associated with program/erase cycling of conventional stacked-gate flash memory, is the overerase phenomenon due to so called "erratic erase" [2]–[4]. Erratic erase shows itself as random, unpredictable variation of cell threshold voltage V_t between consecutive program/erase operations.

Though the physical nature of erratic erase behavior is still questionable, the most widely accepted explanation of this effect is based on anode hole injection (AHI) mechanism [5], [6]. According to AHI model, holes injected to the tunnel oxide during erase operation can be trapped near the floating gate thus increasing electric field and tunneling current during subsequent erase operation. Variation of erase characteristics of the "erratic" cell is therefore thought to be a result of hole trapping/detrapping processes. At the same time, WKB calculations show that the observed V_t variations can not be explained by trapping/detrapping of a single hole; only a cluster of holes (two and more) can result in a measurable modulation of tunneling current during erase of a stacked-gate cell [3], [7].

So far all the publications on erratic erase phenomenon were related to stacked-gate flash memory cells. In this paper a similar effect in SuperFlash® split gate cell is described and analyzed for the first time. The unique structure of SuperFlash® cell, which uses a floating gate (FG) field enhancing tunneling injector [8], allowed us to observe a fine structure of erase instabilities associated with trapping/detrapping of single elementary charges. Whereas the physical mechanisms responsible for erase instabilities observed in both types of flash memories may be different, we believe that our results in some extent can also be applicable for stacked-gate and other floating-gate technologies.

II. EXPERIMENTAL SETUP

The devices used in this work were 32 Mbit arrays fabricated using 0.18 μm self-aligned SST SuperFlash® technology [9]. The structure of SuperFlash® split-gate memory cell is shown in Fig.1. The cell uses interpoly Fowler-Nordheim (F-N) tunneling from FG tip for erase [10] and channel hot-electron injection for programming. During erase a high positive voltage V_{ee} is applied to control gate (wordline), all other cell nodes are grounded. A typical dependence of cell read current I_{cell} vs. FG potential is shown in Fig.2. After regular erase the FG potential is highly positive, and cell current Ir_1 is mainly determined by the control gate transistor. This means that in deep erased state the cell is not sensitive to the FG potential variation which potentially may occur during program/erase cycling. In such a manner integrated control gate provides overerase protection.

In order to increase cell sensitivity to any variations of erase characteristics, we intentionally used lower V_{ee} for erase during program/erase cycling to bring the cell to weakly erased state.

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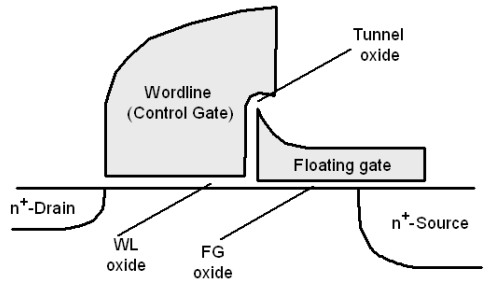

Fig.1. Structure of SuperFlash® cell.

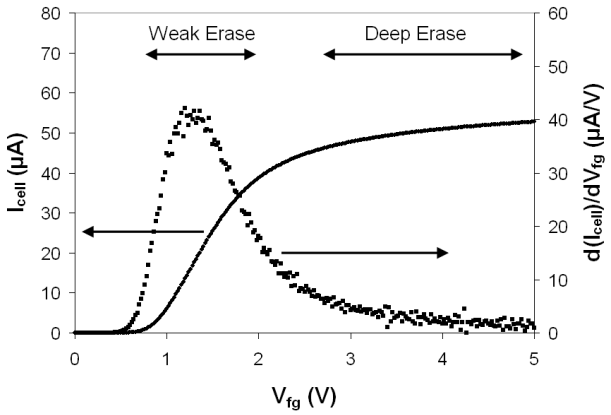

Fig.2. Cell current as a function of FG potential. Data obtained from an isolated cell with a contact to FG. Read conditions: control gate voltage is +3V, drain voltage is +1V.

The measurement of I_{cell} kinetics during cycling included: regular programming, weak erase, and measurement of cell current. This sequence was repeated up to 10,000 times.

To quantify the changes of cell's erase performance we use a concept of erase voltage V_{erase}. We define V_{erase} as a voltage, applied to control gate during erase (at fixed pulse width, e.g., 10 ms), which is required to reach a certain value of I_{cell} at normal read conditions. The example of V_{erase} measured at 50% level of Ir_1 is shown in Fig.3.

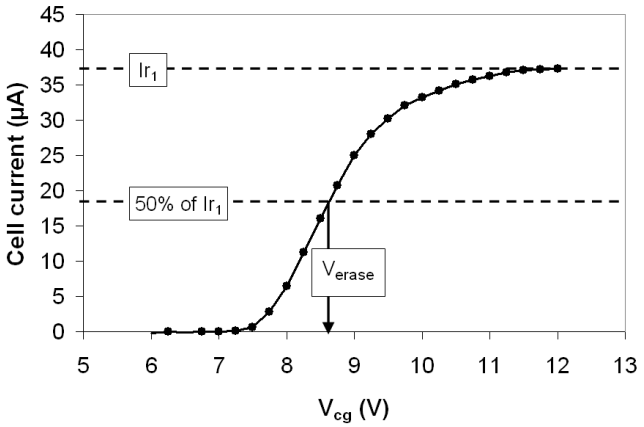

Fig.3 Erase curve of SuperFlash® cell measured at 10 ms erase pulse duration. Cumulative erase mode (no programming between consecutive erase pulses).

III. RESULTS AND DISCUSSION

A. Experimental Results

We measured cell current vs. number of program/weak erase/read cycles for hundreds of cells and found that the vast majority of cells from the memory array shows a well-defined fine structure of cell current kinetics during cycling. Some typical examples of cell current behavior are shown in Fig.4. Degradation of cell's erase performance occurs in steps, each resulting from the trapping of a single electron in the tunnel oxide. In Fig.4(a), for example, one can see 7 electrons trapped during 10,000 program/erase cycles. Some cells show reverse process events – electron detrapping (read current after erase operation, which follows the electron detrapping event, jumps up to its previous level). When the trapping and detrapping frequencies are comparable, an "erratic-like" behavior can be detected – unpredictable fluctuations of erase effectiveness between cycles. When there are two or more electron traps, the picture becomes more complicated (Fig.4(d)).

Note that there are two different sources of erase instabilities (Fig.5). First one, which shows itself as a "white" noise of the I_{cell} baseline, is a result of a shot noise, i.e., fluctuations of the number of tunneling electrons between two consecutive erase operations. This noise is a fundamental property of a tunneling process and can not be reduced for a given number of electrons transferred through the tunnel oxide. The amplitude of shot noise is approximately the same for every cell as long as cells have the same number of electrons extracted from the floating gate during erase (the number of tunneled electrons can be roughly correlated to the FG potential, and hence to the cell current after erase). The observed amplitude of this noise is in a good agreement with the estimated number of tunneled electrons N and expected standard deviation of this value ($\sqrt{N}$). The second source of noise is similar to "random telegraph noise" and is characterized by two well-defined boundary levels of I_{cell}. This noise is attributed to erase process modulation by trapping and detrapping of single elementary charges in the tunnel oxide. Some intermediate levels of I_{cell} can also be observed when trapping or detrapping event occurs somewhere in the middle of the erase operation.

To prove that the trapping/detrapping noise in SuperFlash® cell is really due to electrons, rather than holes, as was observed for stacked-gate flash memory cells [2], the following experiment was conducted. We chose a cell with a well pronounced erase modulation due to elementary charge trapping event (I_{cell} variation was about 10 μA). It can be seen (Fig.6) that the cell returns to its "high conductance" state during the pause between adjacent program/erase pulses. The increase of cell current after the program/erase cycle which follows the pause, indicates that erase becomes more effective, i.e. during the relaxation we actually observe electron detrapping from the previously filled trap in the tunnel oxide.

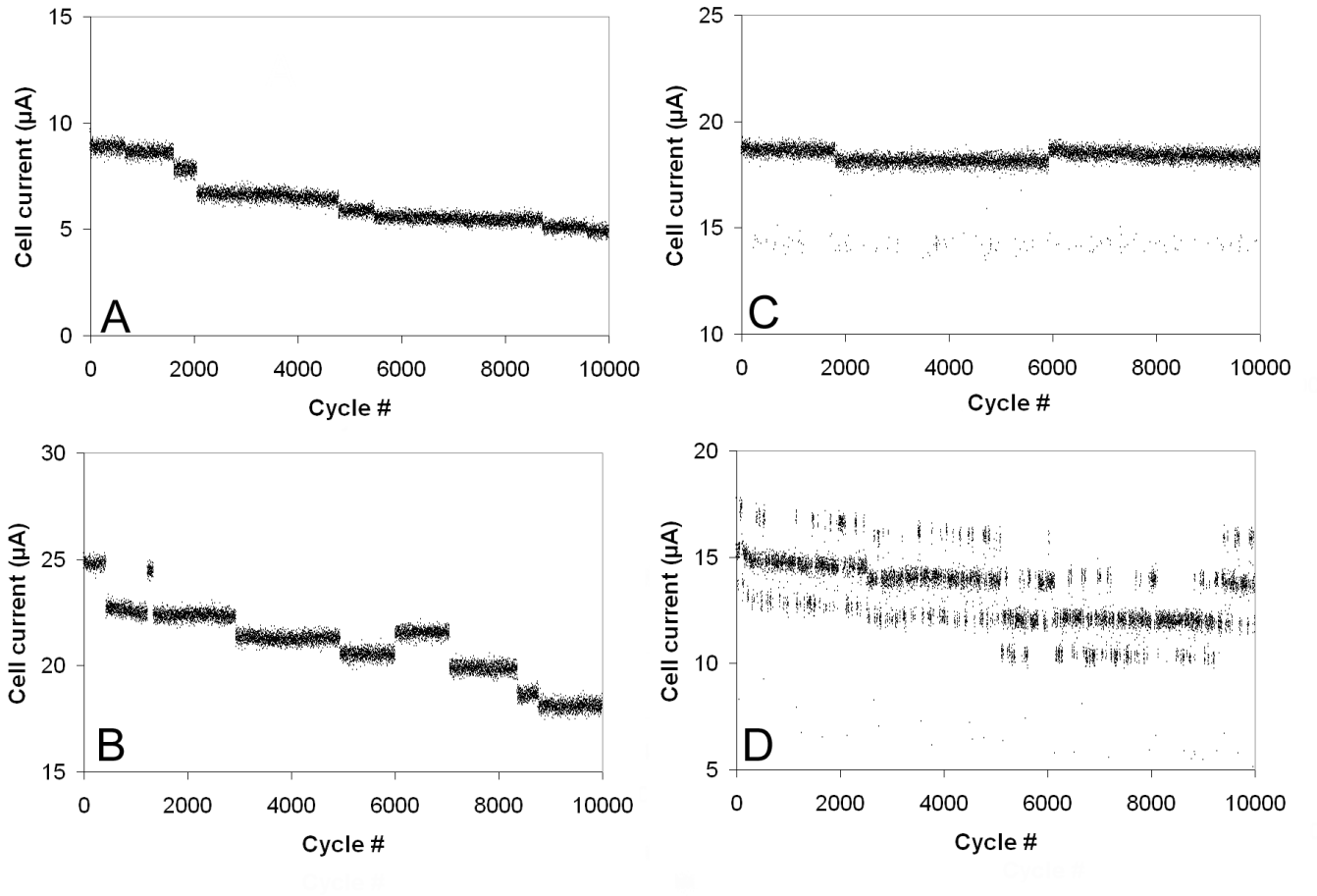

Fig.4. Erase kinetics of cell current during program/erase cycling. Cell current was measured after every erase pulse. V_{ee} was adjusted to bring the cell into weak erase region (see Fig.2).

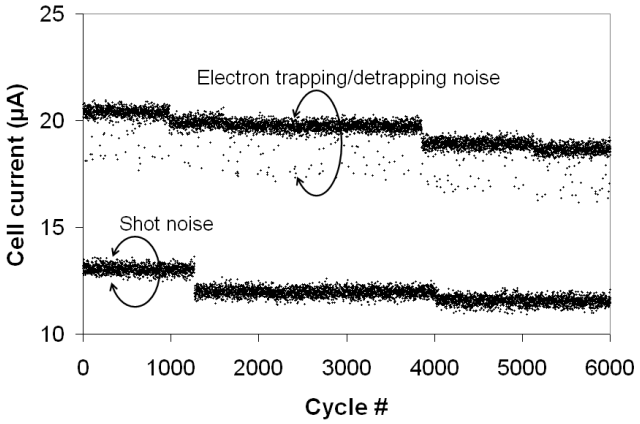

Fig.5. Examples of two sources of erase instabilities – shot noise and electron trapping/detrapping noise

Fig.7 shows a normal probability plot for the amplitude distribution of cell current variation due to single electron trapping/detrapping events. We applied 10 consecutive program/erase cycles to a 4096 cell array, measured cell current after every cycle, and recorded I_{cell} variation for every cell. An average cell current after erase was adjusted to be around 18 μA (50% of Ir_1). As the maximum detectable I_{cell} variation is statistically bounded by half of the entire cell current range ($Ir_1/2$), the obtained distribution is limited by ~18 μA. However, one can use a linear portion of this distribution to estimate the maximum effective I_{cell} variation, which could exist in 32 Mbit array. In our case this variation appeared to be as large as 50 μA. Although such a large I_{cell} variation exceeding Ir_1 can not be directly measured, it can be used to derive the corresponding V_{erase} variation. For 0.18μm cell, 50μA variation of I_{cell} is equivalent to 2.5V change of V_{erase} (see Fig.3). In practice we have observed bits with V_{erase} variation of more than 2V due to single-electron trapping events.

So if we have such a giant effect of single electron on some bits' erase performance, are there any reliability and endurance concerns for SuperFlash® cell? Below are some data showing that in a split-gate cell these effects offer no threat to performance and reliability.

Fig.8 illustrates a correlation between the initial V_{erase} and the frequency of noticeable I_{cell} modulation by single-electron trapping/detrapping events. It can be seen that most cells which show I_{cell} variation of more than 5 μA belong to the fastest portion of the V_{erase} distribution. The initially fastest bits in memory array really show a strong erase modulation by single-electron events (Fig.9). After trapping electron(s), these

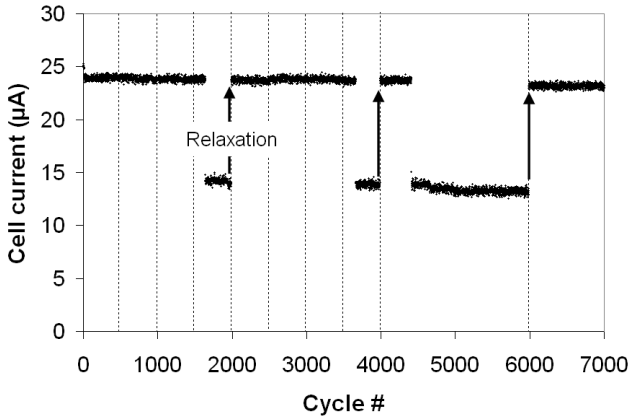

Fig.6. Direction of erase efficiency relaxation. Dashed lines indicate the pauses in cycling procedure (cell was left in erased state for 30 min at room temperature). After one program/erase pulse following the relaxation period, the cell returned to its "high conductance" state.

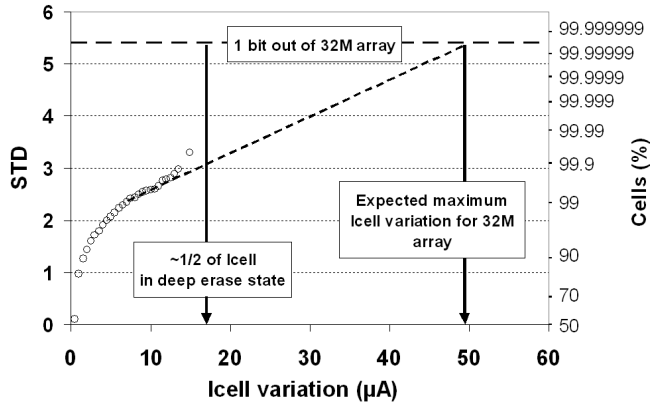

Fig.7. Distribution of the amplitude of I_{cell} variation due to single electron trapping/detrapping events.

cells just become "average" cells from the viewpoint of erase performance.

From our data it can be seen that V_{erase} (and I_{cell}) variations in a SuperFlash® cell are due to electron trapping/detrapping events in the tunnel oxide, rather than hole trapping/detrapping, as it was earlier reported for stacked-gate cells. However, a question regarding the nature and charge state of the traps still remains open. From the general considerations it seems that most electron traps which reveal themselves during our experiments are neutral. If we suggest that the traps are positive, we will come up with unreasonably high density of fixed positive charge in the tunnel oxide (about 10^{13} cm^{-2}), which would have been easily detectable by means of MOS V_t and C-V characteristics. On the other hand, we have strong experimental evidence that some of these electron traps, especially those detected in initially fast cells, are positively charged. Analysis of the charge state of electron traps is beyond the framework of this paper and will be published in the future.

B. Comparison of SuperFlash® and Stacked-Gate Cells

There is a significant difference in the nature of single

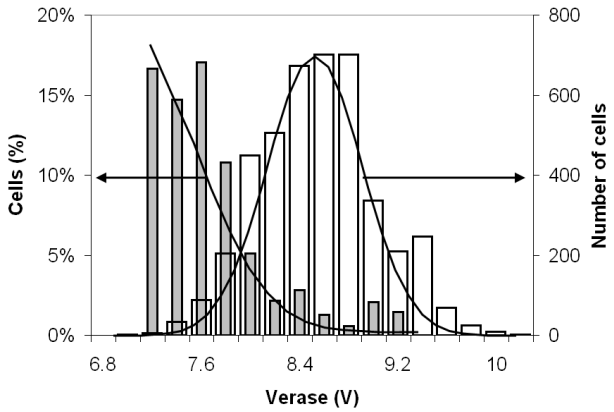

Fig.8. Initial V_{erase} distribution and percentage of cells that show single-electron-induced fluctuations of I_{cell} more than 5 μA. 4096 bits, 10 consecutive program/erase/read cycles.

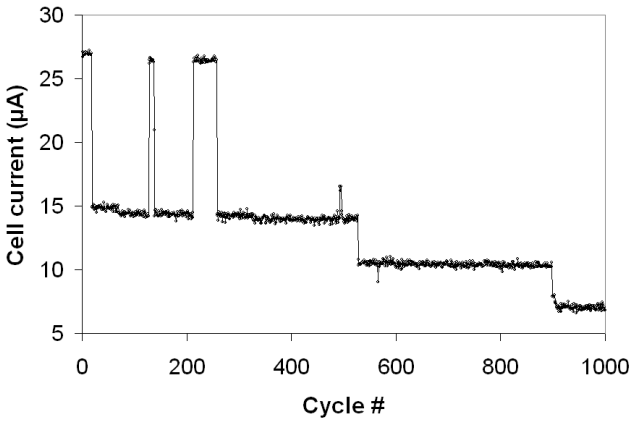

Fig.9. Typical I_{cell} kinetics for a fast bit.

electron/hole trapping events in the tunnel oxide of SuperFlash® and stacked-gate cells, which comes from the difference in cells' structures. In Table 1 we summarized the major observed differences between SuperFlash® and stacked-gate flash cells behavior from the viewpoint of charge trapping in the tunnel oxide.

TABLE I
CHARGE TRAPPING PROCESSES IN TUNNEL OXIDE OF STACKED-GATE AND SUPERFLASH® CELL

	Phenomenon	Stacked-gate cell	SuperFlash® cell
1	Degradation of erase performance during Program/Erase cycling (for an average cell)	Gradual (no fine structure)	Discrete
2	Charge carrier responsible for large modulations of erase performance	Holes	Electrons
3	Anode hole injection mechanism	Yes	Not detected
4	Formation of "fast erase" tail in cell V_t (V_{erase}) distribution during cycling	Yes	No

1. An average stacked-gate flash cell shows a gradual degradation of erase characteristics (gradual increase of cell V_t

in erased state) [2], whereas a SuperFlash® cell has a well-resolved fine structure due to electron trapping in tunnel oxide. This fact is due to a large difference in Fowler-Nordheim injection area between these cells. At the same cell feature size, the area of F-N tunneling in the SuperFlash® cell is about 2 orders of magnitude less than that in the stacked-gate cell, so even that one trapped electron "blocks" a noticeable fraction of tunneling area. In the stacked-gate cell the effect of single-electron trapping is less or comparable with the shot noise, which fundamentally limits the cell's sensitivity to single-electron trapping.

2. It was shown that erase modulation in the SuperFlash® cell is caused by electron trapping and detrapping processes (see Fig.6). Direction of relaxation after "erratic erase" event in stacked-gate cell indicates that large erase modulation may be due to hole trapping/detrapping [2]. Anode hole injection is considered as the most probable source of holes in tunnel oxide in a stacked-gate cell [5], [6].

3. SuperFlash® and stacked-gate cells are expected to show completely different behavior from AHI viewpoint. So far we did not see any evidence of hole injection during erase in SuperFlash® cell. This can be understood from the cell band diagram during erase (Fig.10). We believe that the key reason is the non-planar geometry of SuperFlash® cell's FG injector – with the same electric field at the FG/tunnel oxide interface, the SuperFlash® cell have wider barrier for any potential hole injection from the control gate. The second possible reason is the thicker tunnel oxide as compared to the stacked-gate cell. According to [11], the mean free electron scattering length in the SiO_2 conduction band is in the order of 13Å. As the SuperFlash® cell uses thick tunnel oxide (150-200Å), the tunneled electron should see more scattering events in the tunnel oxide. As a result, the energy distribution of electrons arriving at the anode should be shifted to lower values compared to that in stacked-gate cell, thus decreasing the probability of hot hole generation (and the energy of hot holes which can be potentially generated).

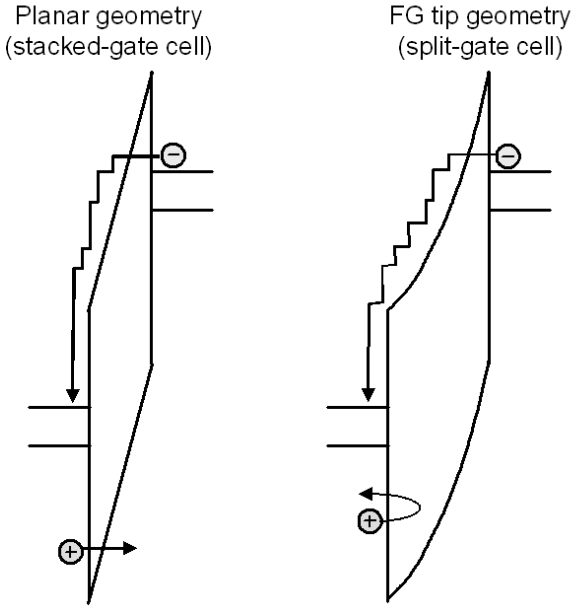

Fig.10. Simplified band diagrams during erase for a stacked-gate and SuperFlash® cell.

4. A large reliability concern for stacked-gate technology is the unpredictability and unscreenability of erratic erase events. The number of erratic bits monotonically increases with the number of program/erase cycles [4]. Eventually every bit may become overerased. Another problem of stacked-gate memories, associated with hole trapping in the tunnel oxide, is cycling-induced read disturb [3]. The SuperFlash® cell may also show some bidirectional modulation of erase performance. But in long-time scale during program/erase cycling, SuperFlash® cells show predictable unidirectional degradation of erase efficiency – we have never observed any cycling-induced enhancement of erase process (Fig.11).

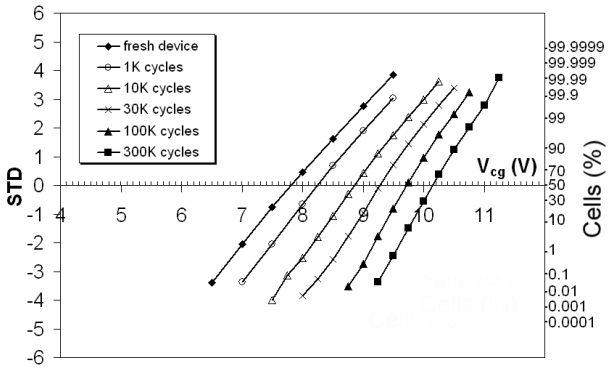

Fig.11. Evolution of V_{erase} distribution during program/erase cycling measured on 32 Kbit sector. There are no endurance failures after 300K program/erase cycles. Note the absence of low-voltage tail formation during cycling.

IV. CONCLUSION

The SuperFlash® cell is shown to be an extremely sensitive instrument for study of single electron trapping/detrapping events in the cell's tunnel oxide. At the same time this cell shows excellent cycling endurance and is inherently protected from overerase due to presence of the control gate. Moreover, as opposed to stacked-gate cell, SuperFlash® cell does not show any cycling-induced formation of "fast erase" bit tail, which we believe is due to the absence of anode hole injection during erase operations.

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