SuperFlash® Memory Program/Erase Endurance

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***Abstract*—**Program/erase endurance data for SuperFlash memory cells are presented. The endurance of SuperFlash products has been greatly improved as tunneling oxide was scaled down. More than 10^6 cycle capability was demonstrated for 32Kbit sector (0.18 µm cell) as compared to 300K endurance for 0.26 µm cell (same sector size). No cycling-induced data retention failures have been detected - 1500 hr bake at 150C revealed no floating gate charge loss on 32Kbit sectors which received $3 \cdot 10^6$ program/erase cycles.

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1. INTRODUCTION

SuperFlash cell is a split-gate EEPROM cell using poly-to-poly Fowler-Nordheim (F-N) tunneling for erase and source-side channel hot electron injection for program [1,2].

SuperFlash cell based on field enhancing electron injector uses a relatively thick oxide for charge transfer during erasing. This greatly extends the vertical scalability of SuperFlash oxides as compared to the thin oxides of the stacked-gate cell.

In this paper we present the results of program/erase endurance study for non self-aligned (0.26 µm and above) and self-aligned (0.18 µm) SuperFlash memory cell generations (Figure 1a,b).

The endurance of flash memory is limited not only by reduction of program/erase efficiency, but also by data retention failures due to stress-induces leakage current (SILC) [3,4]. The average electric field during erase in SuperFlash cell tunnel oxide is about 6-7 MV/cm. This is significantly lower than ≈10 MV/cm used in stacked-gate flash memory. In addition, tunnel oxide in SuperFlash cell is exposed to electric field for significantly less time during erase as compared with the stacked-gate approaches. As for thin FG oxide in SuperFlash, it never sees high (F-N) electric field during cell operation. Therefore SuperFlash cell is less prone to SILC-related data retention failures. Below we will demonstrate the absence of data retention problem caused by erase/program cycling of SuperFlash memory products.

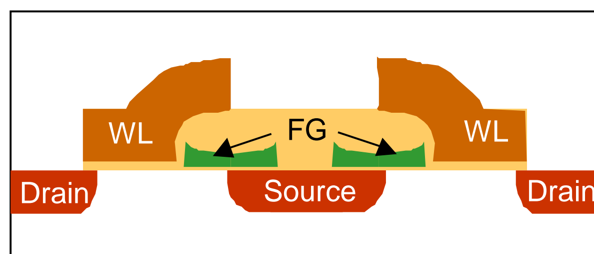

***Figure 1a**. Non self-aligned SuperFlash cell (0.26-µm and above) for low density flash memory.*

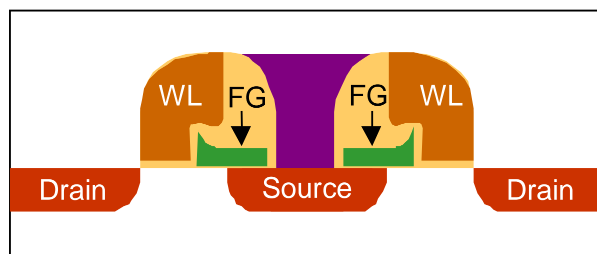

***Figure 1b**. Self-aligned SuperFlash cell (0.18-µm) for high density flash memory.*

2. TUNNEL OXIDE SCALING AND ENDURANCE

Measurements on cell array structures

The dominant mechanism of SuperFlash memory cell degradation under program/erase cycling is electron trapping in tunnel oxide near floating gate injector during erase. Electron trapping occurs on existing traps and traps

generated during cycling. The negative charge around floating gate tip reduces F-N current and erase efficiency.

For quantitative characterization of charge trap-up in tunnel oxide we use the value of forward tunneling voltage (*FTV*) between control gate (Word Line) and floating gate. *FTV* is defined as WL voltage required to maintain certain tunnel current through oxide. Special structure for *FTV* measurement consists of an array of cells with common contact to floating gates. 4K to 9K cell structures are connected in parallel to increase current sensitivity. In our experiment we forced a constant current $3.7\cdot10^{-12}$A per 1μm of floating gate injector length (it has a blade shape) and monitored the voltage difference between WL and floating gate. Figure 2 shows the results of *FTV* degradation measurement at 20°C and 125°C. The cumulative tunneling charge at the end of the tests is $1.85\cdot10^{-9}$ C/μm. It is equivalent to the charge transferred through the tunnel oxide after $(3\div5)\cdot10^{5}$ program/erase cycles. A clear trend of trap-up rate reduction is observed with successively thinner tunnel oxides.

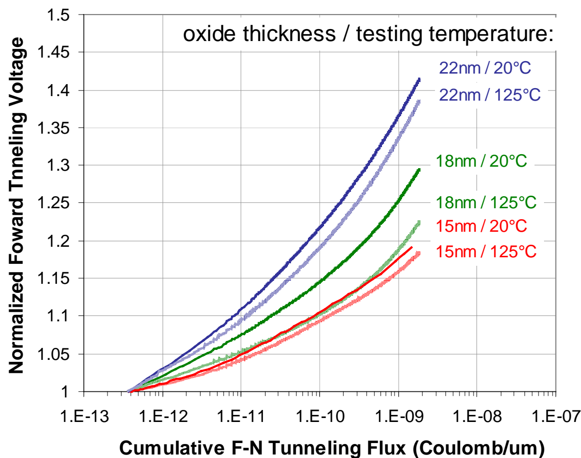

Figure 2*. The increase of FTV under constant current stress in cell arrays with contact to FG for different tunnel oxide thickness at room temperature and 125°C.*

Single cell measurements

In the above experiment we used a constant F-N tunneling current density for different oxide thickness. During realistic erase operation the tunneling current varies with time during erase and the total electron charge transferred from floating gate injector is different for different generations. It is therefore important to compare trap-up rate for functional memory cells from different generations at real-life cycling conditions. For quantitative characterization of trap-up rate in memory cell we use erase voltage value V_e defined as WL erase voltage required to achieve a certain cell current level after erase. V_e directly correlates with *FTV*. Figure 3 demonstrates the relative increase of V_e during program/erase cycling with tunnel oxide thickness for three SuperFlash generations. The result indicates trap-up reduction as the tunnel oxide thickness is scaled down.

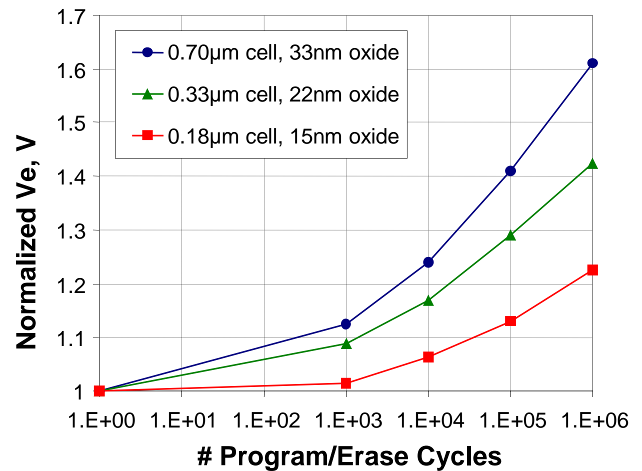

Figure 3*. Normalized erase voltage vs. # of program/ erase cycles.*

3. ENDURANCE EVALUATION TECHNIQUE

Evaluation of product endurance is a time- and resource-consuming procedure. For example, 10^{6} program/erase cycles for the whole 32M memory array takes about a year of continuous cycling. To estimate product endurance in a practical time scale, one has to use some of reliability prediction techniques. These techniques are generally based on cycling of a relatively small portion of memory array and extrapolation of failure probability data to the whole array or to even larger population (wafer, lot, etc.) [5].

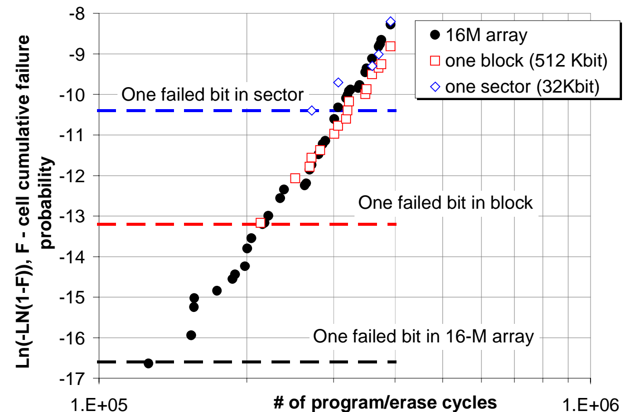

Figure 4*. Weibull plot for 16Mb array endurance distribution based on the whole array cycling. The memory array consists of 32 blocks; each block includes 16x32Kb sectors. 0.26-μm SuperFlash non-self-aligned cell. Fail bit count was collected from the whole array and its different portions at the same time.*

Figure 4 shows cumulative failure probability in Weibull coordinates vs. logarithm of program/erase pulse number. It can be seen that Weibull distribution adequately describes product endurance - data obtained during cycling any portion of the array fall on the same straight line.

Straight line (unimodal Weibull distribution) points to the fact that there is only one failure mode. Therefore the endurance distribution for a large cell population may be reconstructed using endurance distribution for a relatively small portion of the array.

4. ENDURANCE DISTRIBUTION OF MEMORY ARRAY

The product endurance is improved significantly as the tunnel oxide thickness is decreased. More than 1 million program/erase cycle endurance capability has been demonstrated on 32Kb sector based on 0.18-µm cell (Figure 5) as compared to 300K cycle endurance obtained for the same size sector based on 0.26-µm cell (Figure 4).

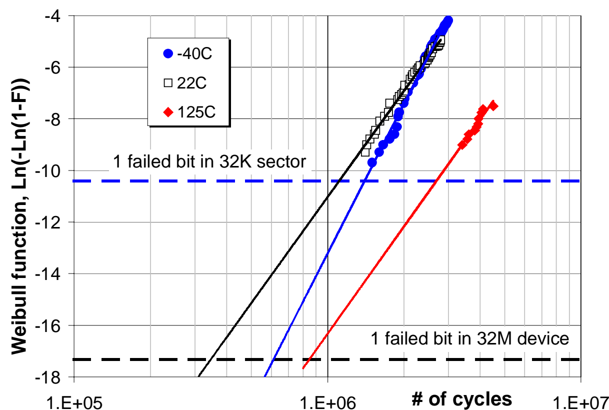

Figure 5*. Weibull plots for endurance distributions measured on 32Kb sectors at three different temperatures. 0.18-µm SuperFlash self-aligned cell.*

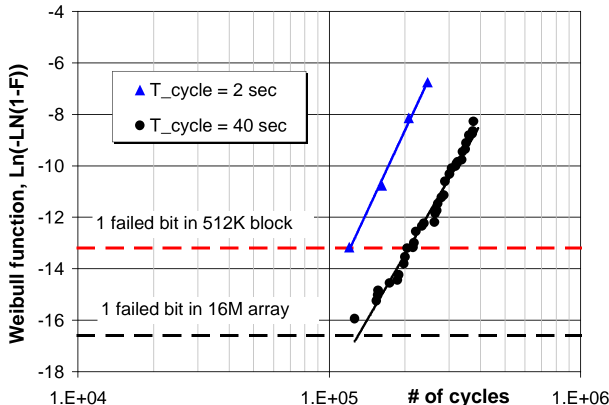

Figure 6*. Endurance improvement due to electron detrapping effect. Device subjected to "slower" cycling shows better endurance. 0.26-µm non-self-aligned cell.*

The data in Figure 5 shows significantly better endurance at elevated temperature. This is due to electron de-trapping in tunnel and floating gate oxides during the quiescent period between erase and program operations. Figure 6 illustrates the effect of cycling frequency on device endurance – device subjected to less frequent program/erase cycling show better endurance. In practice, this means the endurance in most real applications (cycling frequency < 1 cycle/hr) will be at least 2x greater than the endurance demonstrated in a stress environment, where the device is being cycled at the maximum possible frequency.

5. DATA RETENTION AFTER PROGRAM/ERASE CYCLING

Relatively low electric fields used during erase operation reduce the probability of cycling-related data retention failures in SuperFlash products. In fact, oxide leakage mechanism - SILC, which is known to be a reliability concern in stacked-gate cell, so far has not been observed in interpoly oxide of SuperFlash cell [6]. Next advantage is that a thin 8-10nm oxide film underneath the floating gate is never exposed to high F-N fields, thus, showing substantially higher resistance to SILC as compared to the FG oxide in stacked-gate cell.

Data retention test has been performed on array fragments (sectors) containing 32Kbits from three different 0.18-µm devices. Each sector was subjected to 3 million program/erase cycles. After cycling the devices were baked at 150°C and cell current of every bit has been measured. No one leaky bit was found after 1500 hr bake. Cell current distribution for one sector before and after bake is shown in Figure 7. The distribution is slightly and uniformly shifted toward higher current due to effect of electron de-trapping in the floating gate oxide.

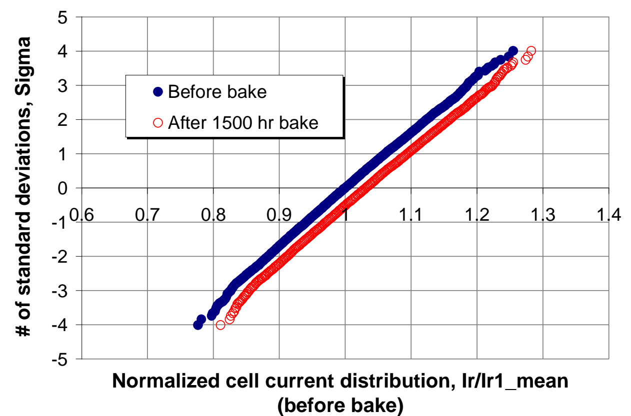

Figure 7*. Normal probability plot for normalized cell current of 32K bits subjected to 3 million program/erase cycles. Distribution was measured before and after 1500-hrs bake at 150C. 0.18-µm SuperFlash self-aligned cell.*

CONCLUSIONS

The endurance of SuperFlash memory is improved significantly as the tunnel oxide is scaled down. More than 1-million program/erase cycle capability at room temperature has been demonstrated for 32Kbit sector (0.18 µm cell) as compared to 300K endurance for 0.26 µm cell (same sector size).

Cycling-induced failure probability distribution shows only one failure mode. This allows us to use endurance evaluation technique based on cycling only a small portion of array and extrapolation of obtained data to a larger cell population (array, wafer or lot scale).

Data retention test performed on three 32Kbit sectors from 0.18-µm devices after 3 million erase/program cycles demonstrated outstanding resistance of SuperFlash to cycling-related data retention failures. No leaky bits have been detected after 1500 hr bake at 150°C.

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