Charge-Gain Program Disturb Mechanism in Split-Gate Flash Memory Cell

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ABSTRACT

Intrinsic charge-gain program disturb mechanism in split-gate flash memory cells has been identified based on simulation results and experimental data obtained on memory arrays fabricated with 0.18 µm SuperFlash® technology. It was shown that program disturb has the same nature under all three program disturb conditions existing in NOR flash memory array, and is a result of band-to-band tunneling caused by high electric field in the split-gate channel area and subsequent hot electron injection. We also analyzed reliability aspects of this program disturb mechanism on 16-Mbit memory arrays, and found no substantial effect of 10^5 program-erase cycles on disturb characteristics. The understanding of intrinsic program disturb mechanism is important for split-gate cell technology scaling as well as for optimization of cell design and operating conditions.

INTRODUCTION

Split-gate memory cells utilizing poly-to-poly tunneling for erasing and source-side hot electron injection for programming [1], [2] are widely used in stand-alone and embedded flash memory because of their superior reliability, manufacturability, low-power operation and over-erase immunity. In split-gate-cell memory arrays, high programming voltage applied to the common source of small-size sector may cause unintentional programming of unselected erased cells (charge-gain program disturb). Several physical mechanisms which can be responsible for program disturb have been discussed in the literature. Data can be lost either due to electron tunneling from word line (WL) to floating gate (FG), referred to as reverse tunneling [3], [4], or due to hot-electron injection which occurs provided there are mobile electrons in the high-field region of the channel area. Previously reported origins of channel mobile electrons under program disturb stress include subthreshold current and gate-induced drain leakage [5]–[7].

To prevent program disturb issues, one should maintain high programming voltage within the program vs. disturb window [8], with reasonable safety margin. As long as programming voltage meets this requirement, program disturb failures are mainly caused by process-induced defects that can be efficiently screened out. For appropriate optimization of cell design and operating conditions, it is therefore essential to understand the physical mechanism which defines program disturb characteristics of cells from the intrinsic population.

In this paper we report a systematic analysis of the program disturb behavior of split-gate flash memory cells under different disturb conditions. Intrinsic charge-gain program disturb mechanism is discussed based on simulation results and experimental data.

EXPERIMENTAL

Measurements were performed on NOR flash memory arrays fabricated using 0.18 µm SST SuperFlash® technology [2]. A schematic cross-section of a SuperFlash® cell along the channel and typical voltages applied to the cell nodes during program and erase operations are shown in Fig. 1. Memory array segment schematic and definition of program disturb conditions are shown in Fig. 2. Depending on the relative location of selected and unselected cells, three program disturb conditions are possible: row disturb, column disturb and diagonal disturb. Typical voltages and stress durations under program and disturb conditions are given in Table I.

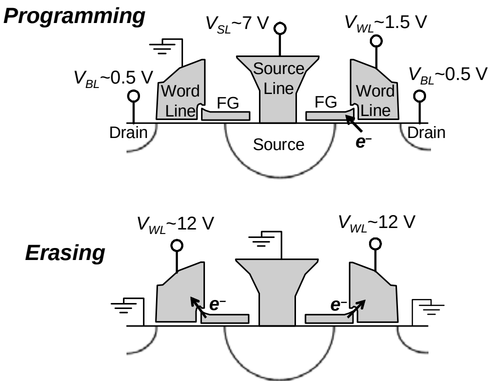

Fig. 1: A schematic cross-section of a SuperFlash® cell along the channel and typical program and erase conditions.

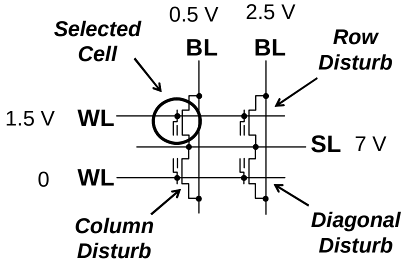

Fig. 2: NOR memory array segment schematic and definition of the three program disturb conditions.

Table I: Typical cell program and disturb conditions.

	SL	BL	WL	Stress duration
Programming	7 V	0.5 V	1.5 V	5 µs
Row disturb		2.5 V	1.5 V	1.25 ms
Diagonal disturb		2.5 V	0	8.7 ms
Column disturb		0.5 V	0	35 µs

To characterize program disturb behavior of individual cells in memory arrays, we measured time-to-failure (*TTF*) disturb characteristics in a wide range of source line (SL) voltages (V_{SL}) for all three program disturb conditions. *TTF* was defined as disturb stress time required to reduce read current of a cell by 1/3 from its initial value after erase.

Medici and TSUPREM-4 were used for 2-D process and device simulation.

RESULTS AND DISCUSSION

TTF disturb characteristics of SuperFlash® cells

Figure 3 shows *TTF* vs. V_{SL} characteristics for two cells under the three program disturb conditions. These two cells are chosen from different portions of the intrinsic mode of the program disturb voltage distribution (designated as Main distribution in Fig.3). We defined program disturb voltage of an individual cell as the minimum SL voltage which causes program disturb in this cell during 10-ms diagonal disturb stress. As can be seen in Fig. 3, *TTF* under all three program disturb conditions exhibits the same exponential dependence on V_{SL}. In other words, the ratios between *TTF* values for different disturb conditions remain essentially constant throughout a wide range of V_{SL}. It is also important to note that the same program disturb behavior is exhibited by both cells chosen from different portions of program disturb voltage distribution. These results suggest that a single physical mechanism controls program disturb under all three program disturb conditions for the entire intrinsic mode of the disturb distribution.

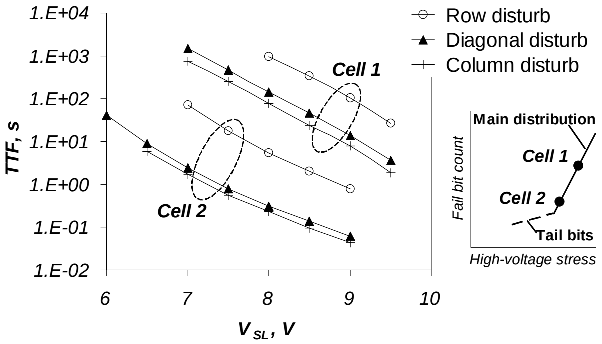

Fig. 3: *TTF* vs. V_{SL} program disturb characteristics for two cells with different disturb rate.

Program disturb mechanisms discussion

In this section we will first review three key program disturb mechanisms reported in the literature, including subthreshold current, reverse tunneling and FG-induced source leakage. The possibility of these mechanisms as origin of intrinsic program disturb will be discussed in the framework of our experimental results. Then we will present simulation data and discuss new program disturb mechanism.

Subthreshold current: Subthreshold current in erased cell under program disturb conditions is determined by WL transistor and therefore very sensitive to WL-BL voltage difference. For program disturb caused by subthreshold current, given the same V_{SL}, one would expect column disturb to be faster than diagonal disturb by many orders of magnitude. This is inconsistent with our observations for the intrinsic cells.

Reverse tunneling: In Fig. 4 we compare *TTF* program disturb characteristics for intrinsic cell and that for a defective cell chosen from the distribution tail. Disturb mechanism for this defective cell was attributed to tunneling of electrons from WL to FG. This was confirmed by SEM pictures (Fig. 5) taken for this cell after electrical failure analysis was completed. The defective cell has irregular WL profile which enhances reverse tunneling. Referring to Fig. 4, diagonal-disturb and column-disturb *TTF* characteristics of defective cell are substantially different from that of normal cell. Besides, diagonal and column disturb in defective cell are considerably faster compared to row disturb (up to 4 orders of magnitude for this particular cell), which is explained by the strong dependence of tunneling current on FG-WL potential difference. Figure 6 illustrates single-electron modulation of program disturb speed in defective cell. Since reverse tunneling is localized at the WL asperity tips, trapping and detrapping of a single electron in tunneling area in oxide results in a visible modulation of disturb speed [9]. At the same time, we have not observed this effect in the intrinsic cells (Fig. 7). This analysis rules out reverse tunneling as a possible mechanism responsible for program disturb in cells from intrinsic mode of distribution.

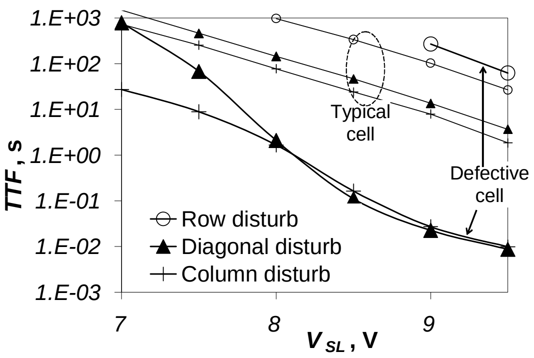

Fig. 4: Typical *TTF* vs. V_{SL} characteristics of cell failed program disturb due to reverse tunneling. Characteristics of typical cell are given for reference.

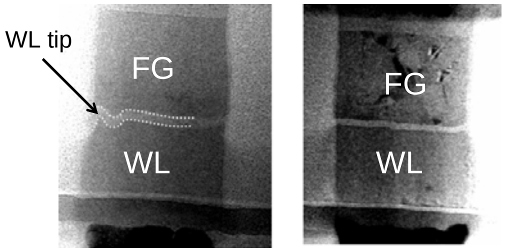

Fig. 5: Top-view SEM pictures of cell which failed program disturb due to reverse tunneling (on the left) and of intrinsic cell (on the right). WL edge irregularity on defective cell is marked by arrow.

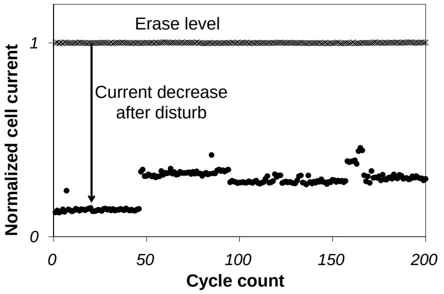

Fig. 6: Single-electron modulation of program disturb rate observed during "erase-program disturb" cycling of cells failed program disturb due to reverse tunneling.

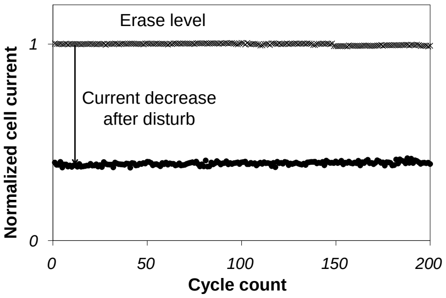

Fig. 7: Single-electron modulation of program disturb rate during "erase-program disturb" cycling is not observed for the intrinsic cells.

FG-induced source leakage: FG-induced source leakage is determined by V_{SL} and FG potential (V_{FG}). It is not sensitive to WL or BL voltages. Therefore, program disturb speed, in terms of V_{FG} vs. time kinetics under disturb stress, if dominated by this mechanism, is not expected to be substantially different for the three program disturb conditions. However, our data for an intrinsic cell (Fig. 8) shows that V_{FG} drops considerably faster under diagonal disturb stress than under row disturb stress. Based on this result, one can conclude that intrinsic program disturb is not caused by FG-induced source leakage.

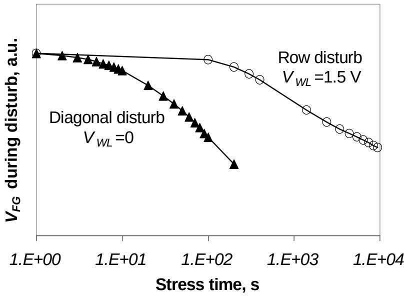

Fig. 8: FG potential (V_{FG}) kinetics under row and diagonal disturb stresses. V_{SL}=8 V.

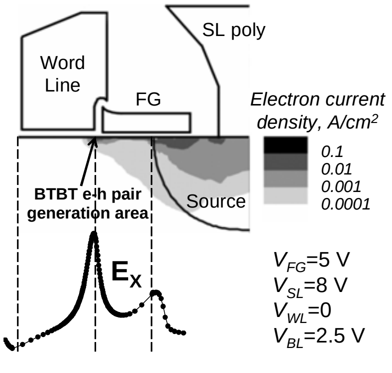

Fig. 9: Simulated 2-D distribution of electron current density in the channel area and distribution of lateral electric field along the channel for diagonal disturb condition.

Simulation results and new program disturb mechanism: Two-dimensional distribution of electron current density in the channel area was simulated for diagonal disturb condition, taking into account BTBT and impact ionization. As is obvious from Fig. 9, electrons which can be accelerated by high lateral electric field and cause program disturb are generated in the split-gate channel area. Simulation showed that the majority of electrons are generated by BTBT, as opposed to impact ionization. Simulated distributions of the lateral electric field in this area for the three disturb conditions are shown in Fig 10. A comparison between data shown in Fig. 3 and 10 testifies good correlation between disturb speed and the maximum channel lateral electric field for the three program disturb conditions. These simulation results fully explain the program disturb behavior of intrinsic memory cells.

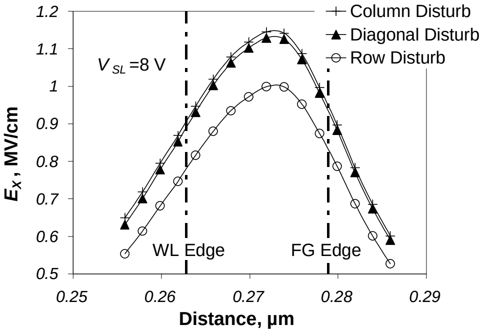

Fig. 10: Simulated distributions of the lateral electric field in the split-gate channel area for the three disturb conditions.

The role of interface states in program disturb

Acceleration of program disturb by hot-carrier stress: Band-to-band carrier generation caused by high electric field can be accelerated in the presence of interface states [10]. To verify the contribution of interface states to program disturb, we measured disturb kinetics of a typical cell before and after continuous hot-carrier stress equivalent to $>10^6$ programming cycles. As evidence of interface state generation, FG transconductance was reduced by ~10% after the stress. As shown in Fig. 11, cell degradation resulted in disturb acceleration by a factor of 100. At the same time, the overall disturb behavior of degraded cell was similar to that of fresh cell, that is, carrier generation in the split-gate area remained a dominant cause of program disturb after hot-carrier stress. Therefore, trap-assisted carrier generation can play an important role in intrinsic program disturb. It should be noted that even after such dramatic cell degradation, *TTF* is still much longer than the actual disturb time cells experience in the memory array.

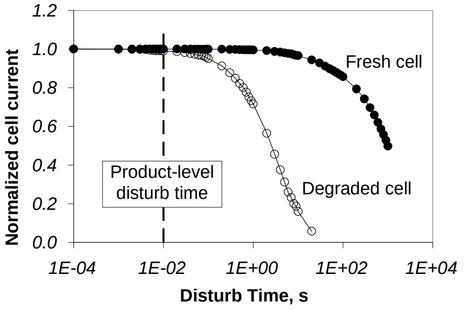

Fig. 11: Acceleration of program disturb after hot-carrier stress. Diagonal disturb condition, V_{SL}=8 V.

Thermal acceleration of program disturb: Arrhenius plots of disturb rate (TTF^{-1}) for diagonal disturb condition in the -40°C to 120°C temperature range are shown in Fig. 12. The slope of the plots becomes steeper with increasing temperature and decreasing V_{SL}. This is an indication of the presence of trap-assisted carrier generation since its relative contribution to BTBT process increases with elevating temperature and lowering electric field [10], [11].

Activation energy of TTF^{-1} evaluated for the 55°C to 120°C temperature range and V_{SL}=7 V is about 0.5 eV. Program disturb mechanism being discussed here is a multi-step process including carrier generation and injection of hot-electrons into the FG. Direct BTBT is relatively insensitive to temperature [6]. Since hot-electron injection efficiency decreases with increasing temperature [12], the overall activation energy of TTF^{-1} is not expected to be higher than that of carrier generation. The observed strong temperature dependence of TTF^{-1} suggests that interface states play an important role in program disturb.

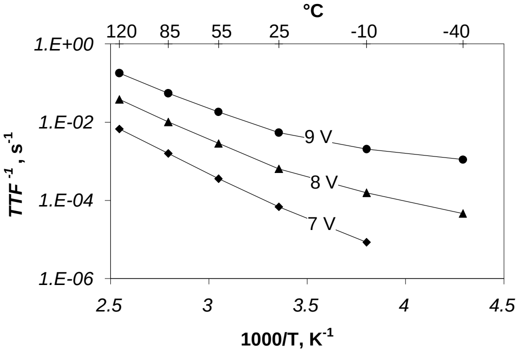

Fig. 12: Arrhenius plots of program disturb rate TTF^{-1} for diagonal disturb mode at different SL voltages.

Reliability aspects of intrinsic program disturb

Product-level program vs. disturb window measured on 16-Mbit NOR memory array fabricated with 0.18 µm SuperFlash® technology provides good margin for programming voltage. We have not observed substantial closure of program vs. disturb window after 10^5 program-erase cycles (Fig. 13). The cells which initially showed the fastest disturb did not become noticeably faster after user-mode cycling. It should be noted that reliability issues related to the generation of tail bits during program-erase cycling, as described earlier in literature [13], in our experience, are the result of excessive program or erase voltage. Such failures can be avoided by proper optimization of operating conditions and cell design.

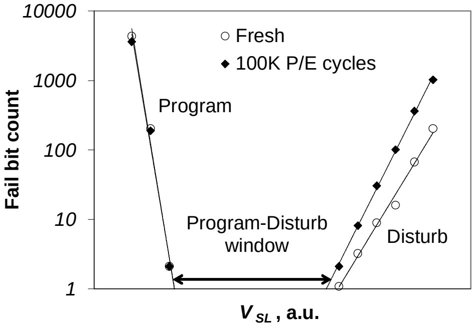

Fig. 13: Program vs. disturb window measured on 16-Mbit NOR memory array before and after 10^5 program-erase cycles.

SUMMARY

A systematic analysis of the intrinsic program disturb behavior of 0.18 µm SuperFlash® memory cells is presented. Simulation data and experimental results show that the disturb mechanism has the same nature for all three different disturb conditions encountered in NOR flash memory array. Disturb was found to be a result of carrier generation by band-to-band tunneling in the split-gate channel area and subsequent heating and injection of these electrons into the floating gate.

Band-to-band tunneling in the split-gate channel area can be accelerated by interface traps, which may be either pre-existent or generated by hot-carrier stress. At the same time, the typical cell has a large disturb "safety margin" and does not experience cycling-induced disturb issues. Array-level program vs. disturb window does not show substantial degradation after 10^5 program-erase cycles.

REFERENCES

[1] S. Kianian, A. Levi, D. Lee, and Y.-W. Hu, "A Novel 3 Volts-Only, Small Sector Erase, High Density Flash E^2PROM", in VLSI Tech. Dig., pp.71-72 (1994)
[2] R. Mih et al., "0.18µm Modular Triple Self-Aligned Embedded Split-Gate Flash Memory", in VLSI Tech. Dig., pp.120-121 (2000)
[3] A. Kotov et al., "Tunneling Phenomenon in SuperFlash® Cell", in NVM Tech. Symp., pp. 110-115 (2002)
[4] C. Y.-S. Cho et al., "A Novel Self-Aligned Highly Reliable Sidewall Split-Gate Flash Memory", IEEE Trans. El. Dev., 53, pp. 465-473 (2006)
[5] D.R. Nair et al., "Drain Disturb During CHISEL Programming of NOR Flash EEPROMs – Physical Mechanisms and Impact of Technological Parameters", IEEE Trans. El. Dev., 51, pp. 701-707 (2004)
[6] L. Chang and J. Lien, "Corner-Field Induced Drain Leakage in Thin Oxide MOSFETs", in IEDM Tech. Dig., pp. 714-717 (1987)
[7] J.-D. Lee, "A New Programming Disturbance Phenomenon in NAND Flash Memory by Source/Drain Hot-Electrons Generated by GIDL Current", in NWSMW Proc., pp 31-33, (2006)
[8] H.-C. Sung et al., "Novel Program versus Disturb Window Characterization for Split-Gate Flash Cell", IEEE El. Dev. Lett, 26, pp. 1-3 (2005)
[9] Yu. Tkachev et al., "Observation of Single Electron Trapping/Detrapping Events in Tunnel Oxide of SuperFlash® Memory Cell", in NVM Tech. Symp., pp. 45-50 (2004)
[10] P.T. Lai et al., "Correlation between Hot-Carrier-Induced Interface States and GIDL Current Increase in N-MOSFET's", IEEE Trans. El. Dev., 45, pp. 521-528 (1998)
[11] M. Rosar, B. Leroy, and G. Schweeger, "A New Model for the Description of Gate Voltage and Temperature Dependence of Gate Induced Drain Leakage (GIDL) in the Electric Field Region", IEEE Trans. El. Dev., 47, pp. 154-160 (2000)
[12] S. Tam, P.-K. Ko, and C. Hu, "Lucky-Electron Model of Channel Hot-Electron Injection in MOSFET's", IEEE Trans. El. Dev., 31, pp. 1116-1125 (1984)
[13] Yu-H. Wang et al., "Novel Cycling-Induced Program Disturb of Split Gate Flash Memory", in IRPS Symp. Proc., pp. 558-563 (2007)