Detection of Single-Electron Transfer Events and Capacitance Measurements in Submicron Floating-Gate Memory Cells

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Abstract—**A simple technique for monitoring floating gate (FG) charge gain/loss with elementary charge accuracy is proposed. The technique does not require nano-scale FG or low temperature and can be applied to virtually any submicron FG memory cell. The potential applications include precise capacitance measurements, as well as analysis of program, erase, disturb and data retention characteristics of FG memory cells in extremely low range of FG current (down to 10^{-23}A and below).**

I. INTRODUCTION

As floating gate (FG) memories are scaled down, the number of electrons representing different logic states of a memory cell reduces [1]. A quantum dot storing a single electron represents the ultimate scaling limit of FG cell. Single-electron transistors (SET) allowing control of single elementary charges on a floating gate (island) have been demonstrated [2], [3]. The manipulation of single electrons in SET is based on Coulomb blockade effect [4] which can be observed when the capacitive charging energy of a floating gate $E=q^2/C_{FG}$ (q=1.6·10^{-19} C) is larger than the thermal energy k_BT. This condition limits the range of FG capacitance and operating temperature of Coulomb blockade-based SET. To observe Coulomb blockade effect at room temperature the FG capacitance C_{FG} should be in the range of 1·10^{-18} F and below, which is achievable in case of nanodot FG [2].

For conventional sub-micron FG memory cells with C_{FG}~1·10^{-16} F the conditions of Coulomb blockade can be achieved at temperatures about 1 K. However these cells are usually considered to be beyond the scope of single-electronics mainly because the variations of FG potential caused by single electrons are too small to result in measurable variations of FG cell threshold voltage (V_t) or cell read current [5].

Whereas Coulomb blockade effect can be used for control of FG charge variations with elementary charge precision, it appears to be possible to monitor these variations even for relatively large (submicron) FG cells which operate far beyond the Coulomb blockade regime.

A simple analysis shows that at C_{FG} =3·10^{-16} F (a reasonable estimate for 0.18 μm NOR flash technology), the variation of FG potential induced by a single electron is about 0.5 mV. Such small changes of FG potential are hardly detectable by means of V_t measurements. However if the FG transistor operates in the subthreshold region with a typical subthreshold swing of 100 mV/dec, same 0.5 mV change of FG potential will result in 1% modulation of transistor current. These variations of FG cell current (for example 100 pA variations at 10 nA baseline) are easily measurable with standard lab equipment.

In this paper we will describe a practical implementation of the above approach which allowed us to detect single-electron transfer in conventional sub-micron floating-gate memory cells at room temperature. We will also demonstrate the applicability of single-electron technique for capacitance measurements in FG cells as well as will mention some other applications of this technique for FG cell characterization and for analysis of charge transfer processes in dielectric layers.

II. EXPERIMENTAL SETUP

A. *Measurement Technique*

The main idea of single-electron transfer detection is in using the sequence of stress and measurement cycles. Here the “stress” means any bias/time conditions which result in the change of FG charge (for example, erase stress, program stress, disturb stress, etc.). The “measurement” is the procedure of measuring cell current in subthreshold region of FG transistor.

To resolve single-electron-induced variations of cell current, the stress conditions should be adjusted in such a way that the probability of single-electron transfer during one stress cycle is relatively small – it should take at least several stress cycles before occurrence of single-electron event. Depending on the stress bias conditions, stress duration may vary in a very wide range (from microseconds to hours). “Measurement” usually does not change the FG charge and therefore integration time can be long enough to provide good measurement accuracy (Fig. 1).

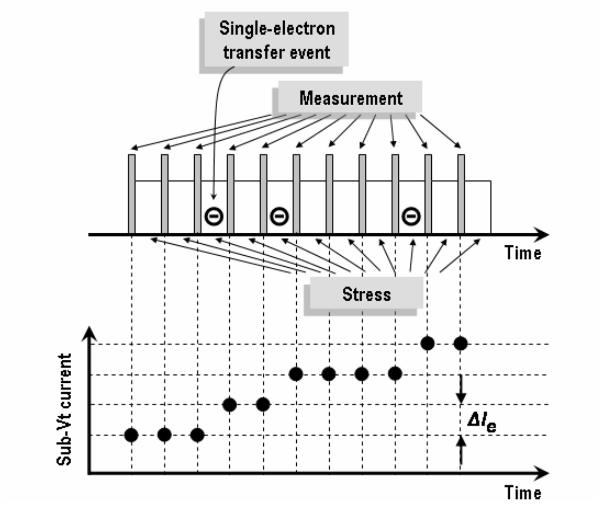

Figure 1. Time diagram of single-electron transfer detection technique.

One particular case which does not require stress and measurement to be separated in time is when stress and measurement conditions are the same. In this case the whole procedure is just a sampling measurement of real-time cell current kinetics. In our earlier work [6] by monitoring cell current during low-voltage erase stress we were able to demonstrate room-temperature real-time single-electron tunneling events in 0.25 µm split-gate FG memory cell.

Note that with this approach the mechanism of electron transfer to/from FG does not necessarily need to be a tunneling process as in case of Coulomb blockade devices. Any current mechanism (hot-electron injection, Shottky emission, stress-induced leakage current, etc.) resulting in FG charge variation can be analyzed with elementary charge accuracy provided that the cell can be brought to FG subthreshold region during cell current measurement.

B. FG Cell Structure and Measurement Setup

For the present work we used a 0.12µm split-gate NOR cell [7], [8]. The cell cross-section is shown in Fig. 2. The cell uses interpoly (Select Gate – FG) tunneling for erase and source-side electron injection for programming. Typical cell program/erase conditions are listed in Table 1.

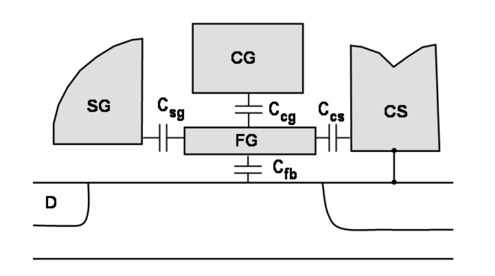

Figure 2. Schematic cross-section of a split-gate cell used in experiments. SG, CG, CS and D denote “Select Gate”, “Coupling Gate”, “Common Source” and “Drain (Bitline – BL)” respectively.

TABLE I. TYPICAL CELL PROGRAM/ERASE CONDITIONS

	WL (SG)	BL (Drain)	CS (Source)	CG
ERASE	11V	0V	0V	0V
PROGRAM (Sel/Unsel)	1.6V/0V	2µA/2.5V	5V/0V	10V/0V

All measurements were performed on an isolated FG cell at room temperature using Agilent 4156C Semiconductor Parameter Analyzer.

C. Observation of Single-Electron Transfer

To bring the cell into FG subthreshold mode, we kept the SG at high potential and biased the coupling gate (CG). Fig. 3 shows the example of single-electron transfer detection during low-voltage erase stress. Cell current modulations due to removal of single electrons from the floating gate are clearly visible As expected for 0.12µm technology node, the amplitude of single-electron modulation is about 1% of the cell current.

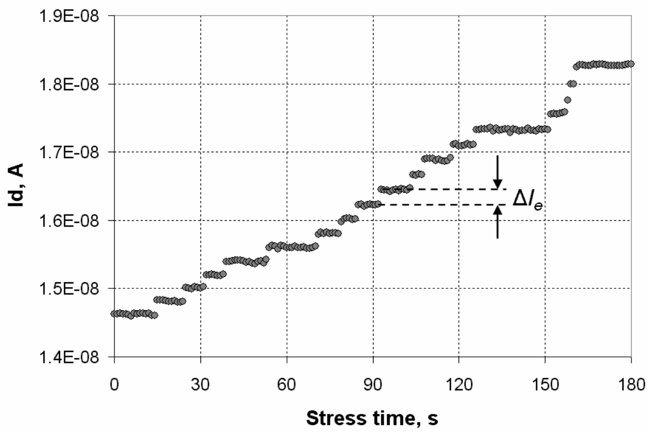

Figure 3. Cell current kinetics during low-voltage erase stress. Stress and measurement conditions are the same: SG/BL/CS/CG=5.8V/0.1V/0V/2V. Sampling interval – 1s.

III. CAPACITANCE MEASUREMENTS

The knowledge of the exact amount of charge transferred to/from FG during single-electron transfer event can be used to calculate the absolute values of cell capacitances with respect to FG.

Floating gate potential equals

$$\varphi_{FG} = \frac{Q_{FG}}{C_{FG}} + \sum_{i=1}^{n} V_i \frac{C_i}{C_{FG}}, \qquad (1)$$

where V_i is the voltage applied to i-th node, C_i is the capacitance between i-th node and FG, C_{FG} is the total FG capacitance.

The change of FG potential caused by a single electron is

$$\Delta\varphi_{FG} = \frac{q}{C_{FG}} \cdot \qquad (2)$$

Same FG potential change can be achieved by changing the potential of the *i*-th electrode

$$\Delta\varphi_{FG} = \Delta V_i \frac{C_i}{C_{FG}} \cdot \qquad (3)$$

Combining (2) and (3), obtain

$$C_i = \frac{qG_i}{\Delta I_e}, \qquad (4)$$

where $G_i = \delta I_d / \delta V_i$ is the cell transconductance measured in operating point (at which cell current I_d is measured), and ΔI_e is the cell current change due to single-electron transfer to/from FG (Fig. 3).

Although equation (4) is very simple, it is not well suited for practical capacitance measurements due to several reasons. First of all, the direct measurements of a single-electron step ΔI_e are not very accurate due to some current noise. Averaging over several steps is not acceptable either because ΔI_e is actually a variable which depends on cell current. The value of transconductance obtained by differentiating the cell's *I-V* curve can also introduce some additional errors in calculation of C_i.

The above problems can however be avoided if we make use of the fact that FG transistor current in subthreshold region is an exponential function of applied gate voltage. In this case ΔI_e is directly proportional to cell current I_d. Introducing a fitting parameter $D = \Delta I_e / I_d$ and a subthreshold swing for *i*-th node S_i (V/decade), we get

$$C_i = \frac{q}{DS_i \log_{10} e} \cdot \qquad (5)$$

Results of step height fitting are shown in Fig. 4. A good fit is obtained using D=1.33·10^{-2}.

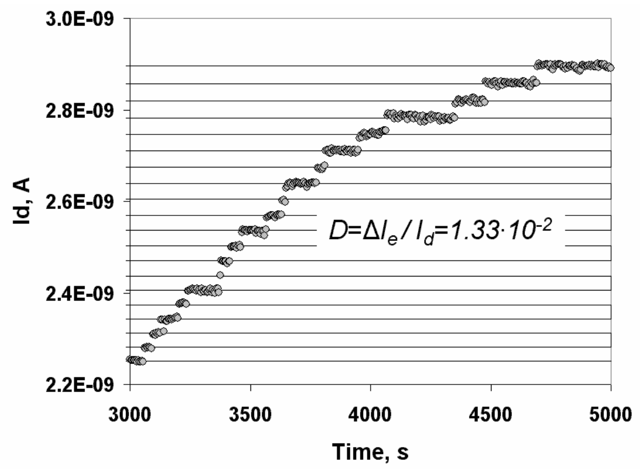

Figure 4. Cell current kinetics during low-voltage erase stress. Horizontal lines show the results of step height fitting.

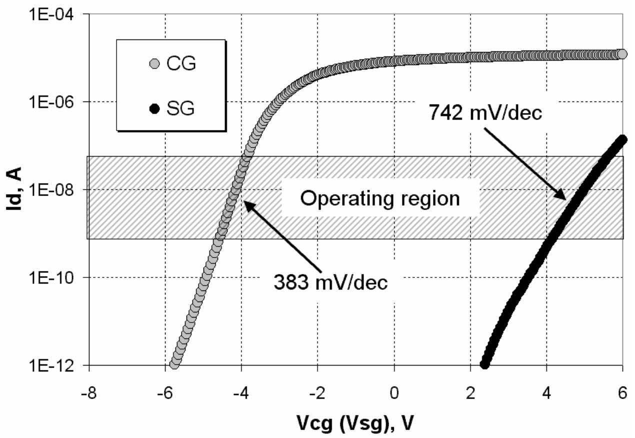

Figure 5. Cell *I-V* characteristics measured with respect to CG and SG.

Using subthreshold swing values for CG and SG (0.383 and 0.742 V/dec, see Fig. 5) we obtain C_{CG} and C_{SG} to be 7.22·10^{-17} and 3.73·10^{-17} F respectively. By measuring the CG-FG coupling ratio [6], [9], which is about 0.38, we are able to calculate the total FG capacitance: C_{FG}=C_{CG}/0.38=1.9·10^{-16} F. It is worth noting that because of the fringing effects, the real FG capacitances obtained using a presented technique are usually higher than the estimates based on the cell physical dimensions.

IV. DISCUSSION

Single-electron transfer events (Fig. 3-4) were detected using sampling cell current measurements. Fig. 6 shows an example of erased cell current kinetics at program disturb conditions. In this case stress and measurement conditions are different. Average interval between single electron transfer events is about 250 ms. During actual program disturb time in NOR flash memory array (~18 ms) the FG is not likely to acquire even one electron, i.e. the cell is very resistant to program disturb.

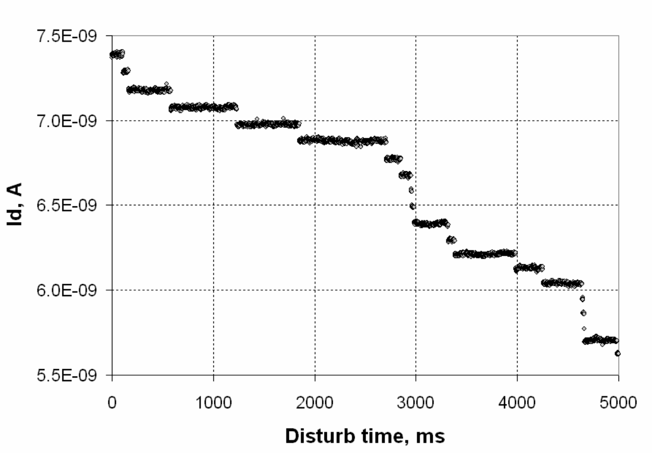

Figure 6. Cell current kinetics during program disturb stress. Disturb conditions: SG/BL/CS/CG=0V/2.5V/5V/10V, read conditions: SG/BL/CS/CG=4V/0.1V/0V/-7.1V. Sampling interval – 1ms.

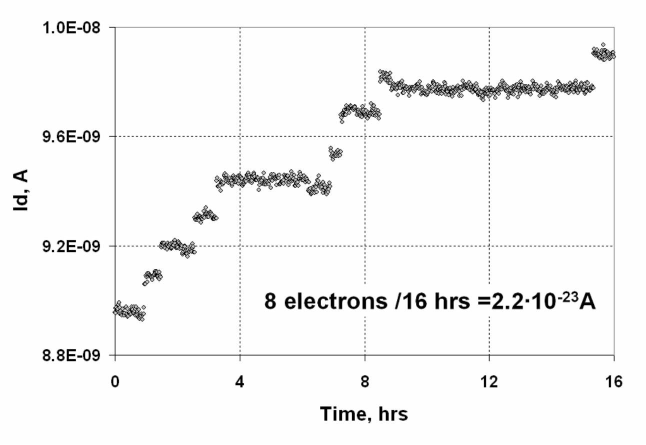

Figure 7. Cell current kinetics during low-voltage erase stress. Stress and read conditions are the same: SG/BL/CS/CG=5V/0.1V/0V/2.9V. Sampling interval – 1min.

As the presented measurement technique is based on the counting of individual electrons, its sensitivity in terms of FG current measurement range is theoretically unlimitedly high. In practice the lower limit of measurable FG current is determined by the equipment long-term stability and by temperature variations during measurements.

Fig. 7 shows cell current during read disturb (low-voltage erase stress). 8 single electron tunneling events have been detected in 16 hours, which is equivalent to an average FG current of $\sim 2.2 \cdot 10^{-23}$ A. The minimum FG current we were able to measure in our experiments corresponds to 1 electron/day ($\sim 2 \cdot 10^{-24}$ A).

The ability to measure vanishingly small real-time FG currents in realistic time frame makes this technique a powerful tool for studying different kinds of disturbs as well as charge retention in FG memories. For example, it can be used to measure *I-V* characteristics of SILC (Stress-Induced Leakage Current) in a range of current, which still guarantees industry-standard 10 years data retention in FG cells (1 electron/day = 3650 electrons/10 years) [1]. Moreover, to our opinion, the sensitivity of this technique is high enough to even resolve "intermediate steps" in cell current kinetics, which may occur when a transferred electron is trapped in dielectric layer or in case of trap-assisted tunneling. In this case by measuring the amplitude of these steps and time intervals between steps one can get information about spatial/energy localization of a single trap and its trapping/emission time parameters.

The technique can also be used for direct measurements of electron counting statistics, and possibly for detection of quasiparticle charges [10], [11].

V. CONCLUSION

We proposed a simple technique for monitoring FG charge variations with elementary charge resolution. The technique can be used for analysis of any mechanism resulting in FG charge gain/loss and can be applied to virtually any submicron FG memory cell provided that the cell can be brought into subthreshold range during cell current measurement.

Possible applications of this technique include:

(a) precise capacitance measurements (for calibration of simulations, failure analysis, circuit design, etc.);
(b) analysis of stress-induced leakage current, study of program/erase/disturbs/data retention in the range of extremely low FG current (down to 10^{-23} - 10^{-24} A);
(c) analysis of electron trapping/detrapping processes and spatial localization of single traps in dielectric layers.

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