SST49LF008A / M50FW080
Firmware Hub Device Comparison

Application Note
April 2008

INTRODUCTION

This Application Note is a comparative list of features for the SST49LF0008A and the ST® M50FW080 Firmware Hub Devices (FWH). Each device is used as BIOS storage and functions as a boot device where the first fetch cycles of the microprocessor are executed.

DESCRIPTION

The following tables detail the features, the software commands, and pin assignments for each device. SST49LF008A uses the JEDEC Software Data Protect (SDP) command set to implement FWH write cycles. The M50FW080 uses a two Bus Write cycle command structure for FWH write cycles.

TABLE 1: Features

Features	SST49LF008A	M50FW080
Block/Sector Definition	64K / 4K	64K / N/A
Command Sequence Cycles	3-6 Write Cycles	2 Cycles
Read/Write Lock Registers	Write Lock / Lock Down	Read Lock / Write Lock / Lock Down
Erase/Program Suspend	No	Yes
Manufacturer ID/Device ID	BFH / 5AH	20H / 2DH
V_{PP} Pin	No	Yes

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TABLE 2: Software Command Cycles

Command Sequence	SST49LF008A	M50FW080
Byte-Program	A0H	40H or 10H
Sector-Erase (4K)	30H	Not Supported
Block-Erase (64K)	50H	20H or D0H
Software ID Entry	90H	90H or 89H
Software ID Exit	F0H	FFH
Read Status Register	Not Supported	70H
Clear Status Register	Not Supported	50H
Program/Erase Suspend	Not Supported	B0H
Program/Erase Resume	Not Supported	D0H

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Pin Assignments

The SST49LF008A V_{PP} pin is not internally connected; whereas, the M50FW080 V_{PP} pin is an optional 12V supply voltage for program and erase operations. Since SST49LF008A requires only a single supply voltage for program and erase operations, driving 12V to this pin has no effect on the device.

The SST49LF008A RB (Ready/Busy) pin is not internally connected and is used in Parallel Programming (A/A Mux Interface) for program/erase completion only during manufacturing programming. SST49LF008A support Data # Polling (DQ7) or Toggle Bit (DQ6) for end of write detection.

SST recommends that all SST49LF008A V_{DD} and V_{SS} Pins be connected for optimal device operations.

TABLE 3: 32-Lead PLCC (NHE)[1, 2]

Pin	SST49LF008A	M50FW080
1	**NC (NC)[3]**	**V_{PP} (V_{PP})**
2	RST# (RST#)	$\overline{RP}$ ($\overline{RP}$)
3	A9 (FGPI3)	A9 (FGPI3)
4	A8 (FGPI2)	A8 (FGPI2)
5	A7 (FGPI1)	A7 (FGPI1)
6	A6 (FGPI0)	A6 (FGPI0)
7	A5 (WP#)	A5 ($\overline{WP}$)
8	A4 (TBL#)	A4 ($\overline{TBL}$)
9	A3 (ID3)	A3 (ID3)
10	A2 (ID2)	A2 (ID2)
11	A1 (ID1)	A1 (ID1)
12	A0 (ID0)	A0 (ID0)
13	DQ0 (FWH0)	DQ0 (FWH0)
14	DQ1 (FWH1)	DQ1 (FWH1)
15	DQ2 (FWH2)	DQ2 (FWH2)
16	V_{SS} (V_{SS})	V_{SS} (V_{SS})
17	DQ3 (FWH3)	DQ3 (FWH3)
18	DQ4 (RES)	DQ4 (RFU)
19	DQ5 (RES)	DQ5 (RFU)
20	DQ6 (RES)	DQ6 (RFU)
21	DQ7 (RES)	DQ7 (RFU)
22	**NC (NC)**	**$R\overline{B}$ (RFU)**
23	WE# (FWH4)	$\overline{W}$ (FWH4)
24	OE# (INIT#)	$\overline{G}$ ($\overline{INIT}$)
25	V_{DD} (V_{DD})	V_{CC} (V_{CC})
26	**NC (NC)**	**V_{SS} (V_{SS})**
27	NC (NC)	NC (NC)
28	**V_{SS} (V_{SS})**	**NC (NC)**
29	IC (IC)	IC (IC)
30	A10 (FGPI4)	A10 (FGPI4)
31	R/C# (CLK)	$R\overline{C}$ (CLK)
32	V_{DD} (V_{DD})	V_{DD} (V_{DD})

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1. ( ) = Designates Firmware Hub Mode
2. NC = not internally connected
3. Bold = Cross product pin inconsistencies

TABLE 4: 32-Lead TSOP (WHE)[1, 2]

Pin	SST49LF008A	M50FW080
1	NC (NC)	NC (NC)
2	NC (NC)	NC (NC)
3	NC (NC)	NC (NC)
4	**V_{SS} (V_{SS})[3]**	**NC (V_{SS})**
5	IC (IC)	IC (IC)
6	A10 (FGPI4)	A10 (FGPI4)
7	R/C# (CLK)	$R\overline{C}$ (CLK)
8	V_{DD} (V_{DD})	V_{CC} (V_{CC})
9	**NC (NC)**	**V_{PP} (V_{PP})**
10	RST# (RST#)	$\overline{RP}$ ($\overline{RP}$)
11	A9 (FGPI3)	A9 (FGPI3)
12	A8 (FGPI2)	A8 (FGPI2)
13	A7 (FGPI1)	A7 (FGPI1)
14	A6 (FGPI0)	A6 (FGPI0)
15	A5 (WP#)	A5 ($\overline{WP}$)
16	A4 (TBL#)	A4 ($\overline{TBL}$))
17	A3 (ID3)	A3 (ID3)
18	A2 (ID2)	A2 (ID2)
19	A1 (ID1)	A1 (ID1)
20	A0 (ID0)	A0 (ID0)
21	DQ0 (FWH0)	DQ0 (FWH0)
22	DQ1 (FWH1)	DQ1 (FWH1)
23	DQ2 (FWH2)	DQ2 (FWH2)
24	V_{SS} (V_{SS})	V_{SS} (V_{SS})
25	DQ3 (FWH3)	DQ3 (FWH3)
26	DQ4 (RES)	DQ4 (RFU)
27	DQ5 (RES)	DQ5 (RFU)
28	DQ6 (RES)	DQ6 (RFU)
29	DQ7 (RES)	DQ7 (RFU)
30	**V_{DD} (V_{DD})**	**NC (NC)**
31	WE# (FWH4)	$\overline{W}$ (FWH4)
32	OE# (INIT#)	$\overline{G}$ ($\overline{INIT}$)

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1. ( ) = Designates Firmware Hub Mode
2. NC = not internally connected
3. Bold = Cross product pin inconsistencies

TABLE 5: 40-Lead TSOP (EIE)[1, 2]

Pin	SST49LF008A	M50FW080
1	NC (NC)	NC (NC)
2	IC (IC)	IC (IC)
3	NC (NC)	NC (NC)
4	NC (NC)	NC (NC)
5	NC (NC)	NC (NC)
6	NC (NC)	NC (NC)
7	A10 (FGPI4)	A10 (FGPI4)
8	NC (NC)	NC (NC)
9	R/C# (CLK)	R$\overline{C}$ (CLK)
10	V_{DD} (V_{DD})	V_{CC} (V_{CC})
11	**NC (NC)[3]**	**V_{PP} (V_{PP})**
12	RST# (RST#)	$\overline{RP}$ ($\overline{RP}$)
13	NC (NC)	NC (NC)
14	NC (NC)	NC (NC)
15	A9 (FGPI3)	A9 (FGPI3)
16	A8 (FGPI2)	A8 (FGPI2)
17	A7 (FGPI1)	A7 (FGPI1)
18	A6 (FGPI0)	A6 (FGPI0)
19	A5 (WP#)	A5 ($\overline{WP}$)
20	A4 (TBL#)	A4 ($\overline{TBL}$))
21	A3 (ID3)	A3 (ID3)
22	A2 (ID2)	A2 (ID2)
23	A1 (ID1)	A1 (ID1)
24	A0 (ID0)	A0 (ID0)
25	DQ0 (FWH0)	DQ0 (FWH0)
26	DQ1 (FWH1)	DQ1 (FWH1)
27	DQ2 (FWH2)	DQ2 (FWH2)
28	DQ3 (FWH3)	DQ3 (FWH3)
29	V_{SS} (V_{SS})	V_{SS} (V_{SS})
30	V_{SS} (V_{SS})	V_{SS} (V_{SS})
31	**NC (NC)**	**V_{CC} (V_{CC})**
32	DQ4 (RES)	DQ4 (RFU)
33	DQ5 (RES)	DQ5 (RFU)
34	DQ6 (RES)	DQ6 (RFU)
35	DQ7 (RES)	DQ7 (RFU)
36	**NC (NC)**	**R$\overline{B}$ (RFU)**
37	OE# (INIT#)	$\overline{G}$ ($\overline{INIT}$)
38	WE# (FWH4)	$\overline{W}$ (FWH4)
39	V_{DD} (V_{DD})	V_{CC} (V_{CC})
40	V_{SS} (V_{SS})	V_{SS} (V_{SS})

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1. ( ) = Designates Firmware Hub Mode
2. NC = not internally connected
3. Bold = Cross product pin inconsistencies

CONCLUSION

There are slight differences between the SST49LF008A and the M50FW080 devices. See *SST49LF008A 8 Mbit Firmware Hub Data Sheet* for detailed information on the device features.

SST49LF008A software drivers are supported by most industry leading BIOS vendors making BIOS and programming support readily available.

The ST is registered trademark of STMicroelectronics. STMicroelectronics M50FW080 data used in this document was taken from the M50FW080 data sheet, revision 10.