

Designing in SST's Multi-Purpose Flash Plus (39 Series) Products



Application Note
November 2005

INTRODUCTION

SST's Multi Purpose Flash Plus (MPF+) family includes all the features and benefits of MPF products, plus four additional features: Erase-Suspend/Erase-Resume, Boot Block, Security ID, and Hardware Reset. In addition, MPF+ products can be designed into systems that use competing devices by implementing appropriate minor hardware and software changes. Although the technical considerations in this application note are based on comparisons with parts from AMD, ST Microelectronics, Macronix, and Atmel, the information could also apply to products from additional companies.

TABLE 1: CROSS REFERENCE TABLE FOR MPF+ FAMILY

Vendor	16 Mbit ¹	32 Mbit	64 Mbit
SST	SST39VF1681, SST39VF1682, SST39VF160x	SST39VF320x	SST39VF640x, SST39VF640xB
AMD	Am29LV160x	Am29LV320x, S29GL032x ²	Am29LV640Mx, S29GL064x ³
ST Micro	M29W160x	M29W320x	M29W640x
Macronix	MX29LV160xx	MX29LV320Ax	MX29LV640x
Atmel	AT49BV162A	AT49BV322Ax	

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1. The SST39VF1681 (bottom boot block protection) and SST39VF1682 (top boot block protection) are 16 Mb devices that are 8 bits wide. The SST39VF160x devices are 16 bits wide.
2. The S29GL032x device has 8 models. SST39VF320x are compatible with S29GL032x models R1, R2, R3, R4, and R5. Model R0 is a x8 device. Models R6 and R7 have a slightly different address pin locations versus SST39VF320x. SST39VF320x complies with JEDEC standard pin assignments.
3. The S29GL064x device has 8 models. SST39VF640x and SST39VF640xB are compatible with S29GL064x models R1, R2, R3, R4, and R5. Model R0 is a x8 only device. Models R6 and R7 have a slightly different address pin locations versus SST39VF640x and SST39VF640xB. SST39VF640x and SST39VF640xB comply with JEDEC standard pin assignments.

Hardware Considerations

The MPF+ family supports the JEDEC standard flash EEPROM pin assignments. As a result, only a few hardware differences need to be kept in mind.

Pin Assignment

SST's TSOP and BGA pin assignments are fully compatible with the devices in Table 1, with the exception of several infrequently used features (Ready/Busy, Accelerated Programming, Individual Block Locking, and Unlock Bypass) not supported by SST.

On MPF+ devices, Pin 12 and Pin 14 (RST#, WP#) have internal pull-up resistors. Hence, if an existing socket has a NC in either of those positions, MPF+ devices are compatible because RST# and WP# will be automatically disabled. These pull-ups also enable backward compatibility with corresponding 16 Mb MPF devices from SST.

Instead of offering a BYTE# pin, SST offers dedicated x8 MPF+ devices, the SST39VF1681 and SST39VF1682. On competing parts, the BYTE# pin is used to select a x8 configuration.

Note: In x8 mode, competitors' addresses may start at A1, which is the same as SST's address bit A0.

TSOP package sizes are also compatible while the BGA package has a few advantageous differences.

BGA ball size and pitch

SST's TFBGA has the same 0.8 mm pitch as other vendors. However, their parts may have smaller ball opening sizes than SST's. In such cases, simply enlarging the ball landing pads to fit SST's larger balls will improve solder joint reliability.

BGA package size

SST parts should easily fit into existing sockets. SST's BGA packages not only maintain the same pin assignments as alternative solutions, but also are up to 40% smaller in size. This size advantage is especially ideal for space constrained applications.

Power-up and Power-down

The following diagram is the recommended power-down and power-up waveform for SST's MPF+ family of devices.



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TABLE 2: RECOMMENDED POWER-UP/DOWN LIMITS

Symbol	Parameter	Limits			Conditions
		Min	Max	Units	
T_{PF}	V_{DD} Falling Time	3	300	ms	90% to 10% of V_{DD}
T_{PR}	V_{DD} Rising Time	0.1	300	ms	10% to 90% of V_{DD}
T_{OFF}	V_{DD} Off Time	100		ms	
V_{OFF}	V_{DD} Off Level		0.3	V	0V (recommended)

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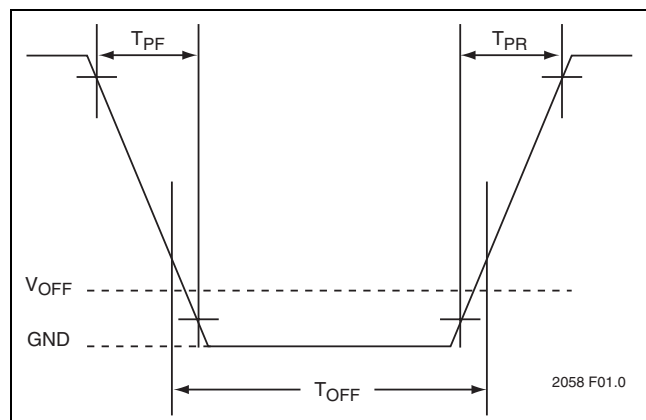


FIGURE 1: RECOMMENDED POWER-UP/DOWN WAVEFORM

Software Considerations

The MPF+ family supports the 6-cycle JEDEC standard command set. As a result, only a few software differences need to be kept in mind.¹

Boot Block

SST has uniform sector size, including the boot block (64 KByte). Others often have asymmetrical boot block sizes.

CFI Query Entry

SST's CFI Query Entry is a three-cycle command, while other vendors use one cycle.

Command Code Address Bits

Consistent with the JEDEC standard, the SST39VF640xB x16 products offer software command sequence compatibility using an 11-bit address format, A_{10} - A_0 .

SST39VF160x/320x/640x x16 products use four additional address bits for each command cycle (e.g. 5555H versus 555H; 2AAAH versus 2AAH). The additional bits improve the intrinsic reliability of the Software Data Protection.

Device ID

SST devices have different manufacturer IDs and Device IDs than the alternatives.

Sector/Block-Erase Command

The 64-KByte Block-Erase command (30H) used by the SST39VF640xB x16 and the SST39VF168x x8 products is compatible with alternative vendors' devices. These products also offer a 4-KByte Sector-Erase command which uses 50H in the sixth cycle, but the smaller sector size may require additional software changes.

Please note that the SST39VF160x/320x/640x x16 products use 50H in the sixth cycle for the 64-KByte Block-Erase command and 30H for the 4-KByte Sector-Erase command.

Security ID

Some vendors do not support Security ID and others may have a different Security ID address space.

SUMMARY

Taking advantage of the benefits of the MPF+ family and SuperFlash technology can be easily done. With the appropriate hardware and software adjustments outlined in this note, the MPF+ family can be the right replacement solution in any design.

1. Alternative products that support Intel's 2-cycle command set require significant changes to software and board layout.