4 Mbit LPC Flash

SST49LF040B

EOL Data Sheet

FEATURES:

- **4 Mbit SuperFlash Memory Array for Code or Data Storage**
  - SST49LF040B: 512K x8 (4 Mbit)
- **Conforms to Intel LPC Interface Specification**
  - Supports Single-Byte LPC Memory Cycle
- **Flexible Erase Capability**
  - Uniform 4 KByte sectors
  - Uniform 64 KByte overlay blocks
  - Chip-Erase for PP Mode Only
- **Single 3.0-3.6V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption**
  - Active Read Current: 6 mA (typical)
  - Standby Current: 10 µA (typical)
- **Fast Sector-Erase/Byte-Program Operation**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Chip-Erase Time: 70 ms (typical)
  - Byte-Program Time: 14 µs (typical)
  - Chip Rewrite Time: 8 seconds (typical)
  - Single-pulse Program or Erase
  - Internal timing generation
- **Two Operational Modes**
  - Low Pin Count (LPC) interface mode for in-system operation
  - Parallel Programming (PP) mode for fast production programming
- **LPC Interface Mode**
  - LPC bus interface supporting byte Read and Write
  - 33 MHz clock frequency operation
  - WP# and TBL# pins provide hardware write protection for entire chip and/or top Boot Block
  - Block Locking Registers for individual block Write-Lock and Lock-Down protection
  - JEDEC Standard SDP Command Set
  - Data# Polling and Toggle Bit for End-of-Write detection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection
- **Parallel Programming (PP) Mode**
  - 11-pin multiplexed address and 8-pin data I/O interface
  - Supports fast In-System or PROM programming for manufacturing
- **CMOS and PCI I/O Compatibility**
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST49LF040B flash memory devices are designed to interface with host controllers (chipsets) that support a low-pin-count (LPC) interface for BIOS code storage. Two interface modes are supported by the SST49LF040B: LPC Memory mode for in-system operation compatible with Intel's LPC Interface Specification and Parallel Programming (PP) mode to interface with industry-standard programming equipment.

The SST49LF040B flash memory devices are manufactured with SST's proprietary, high-performance SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain greater reliability and manufacturability compared with alternative approaches. The SST49LF040B devices significantly improve performance and reliability, while lowering power consumption. The SST49LF040B devices write (Program or Erase) with a single 3.0-3.6V power supply.

The SST49LF040B use less energy during Erase and Program than alternative flash memory technologies. The total energy consumed is a function of the applied voltage, current and time of application. Since for any given voltage range the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

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The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. This means the system software or hardware does not have to be calibrated or correlated to the cumulative number of Erase cycles as is necessary with alternative flash memory technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

The SST49LF040B devices provide a maximum Byte-Program time of 20 µsec. The entire memory can be erased and programmed byte-by-byte typically in 8 seconds for the SST49LF040B device, when using status detection features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent writes, the SST49LF040B device employ on-chip hardware and software data protection (SDP) schemes. It is offered with a typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

To meet high density, surface mount requirements, the SST49LF040B devices are offered in 32-lead PLCC and a 32-lead TSOP package. In addition, SST is providing lead-free (non-Pb) package options to address the growing need for non-Pb solutions in electronic components. Non-Pb package versions can be obtained by ordering products with a package code suffix of “E” as the environmental attribute in the product part number. See Figures 2 and 3 for pin assignments and Table 1 for pin descriptions.

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FUNCTIONAL BLOCKS

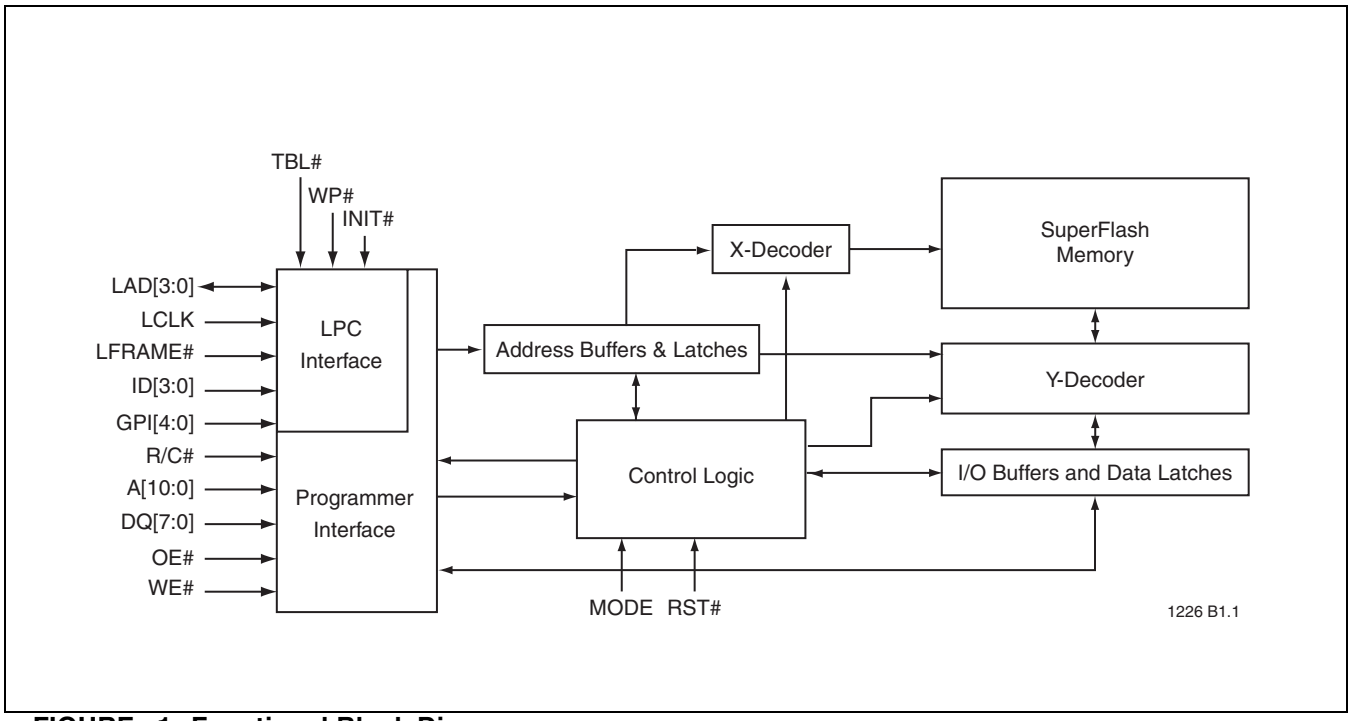

FIGURE 1: Functional Block Diagram

PIN ASSIGNMENTS

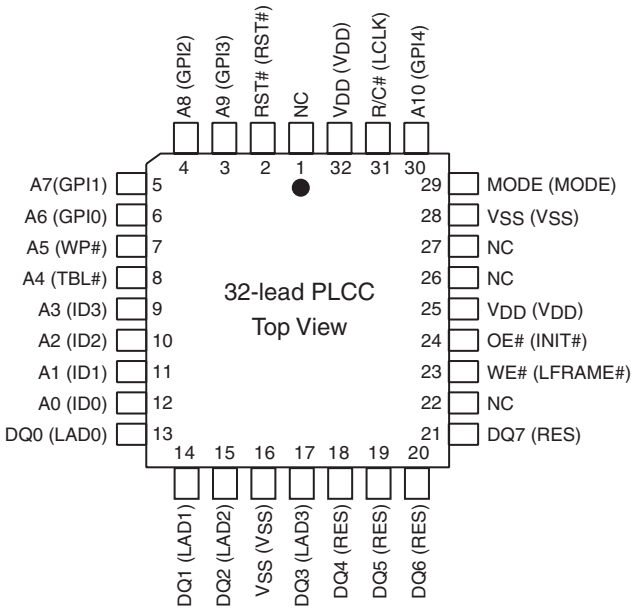

FIGURE 2: Pin Assignments for 32-lead PLCC

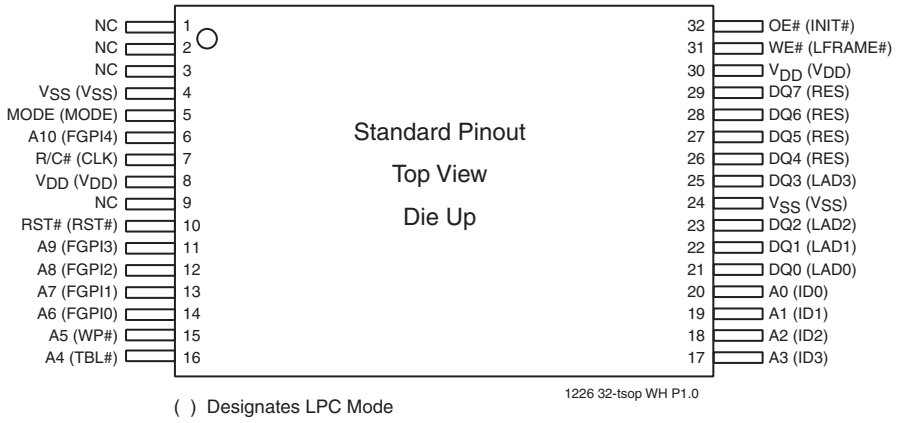

FIGURE 3: Pin Assignments for 32-lead TSOP (8mm x 14mm)

PIN DESCRIPTIONS

TABLE 1: Pin Description

Symbol	Pin Name	Type[1]	Interface PP	Interface LPC	Functions
LCLK	Clock	I		X	To provide a clock input to the control unit. The clock conforms to the PCI specification.
LAD[3:0]	Address and Data	I/O		X	To provide LPC bus information such as addresses and command inputs/outputs to memory.
LFRAME#	Frame	I		X	To indicate start of a data transfer operation; also used to abort an LPC cycle in progress.
MODE	Interface Mode Select	I	X	X	This pin determines which interface is operational. When held high, programmer mode is enabled and when held low, LPC mode is enabled. This pin must be set at power-up or before returning from reset and must not change during device operation. This pin must be held high (V_{IH}) for PP mode and low (V_{IL}) for LPC mode. This pin is internally pulled-down with a resistor between 20-100 KΩ.
RST#	Reset	I	X	X	To reset the operation of the device
INIT#	Initialize	I		X	This is the second reset pin for in-system use. This pin functions identically to RST#.
ID[3:0]	Identification Inputs	I		X	These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0]=0000, all subsequent devices should use sequential count-up strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ.
GPI[4:0]	General Purpose Inputs	I		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read through GPI_REG (General Purpose Inputs Register). These inputs should be at their desired state before the start of the LPC clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated.
TBL#	Top Block Lock	I		X	When low, prevents programming to the boot block sectors at the top of the device memory. When TBL# is high it disables hardware write protection for the top block sectors. This pin cannot be left unconnected.
WP#	Write Protect	I		X	When low, prevents programming to all but the highest addressable blocks. When WP# is high it disables hardware write protection for these blocks. This pin cannot be left unconnected.
R/C#	Row/Column Select	I	X		Select for the Programming interface, this pin determines whether the address pins are pointing to the row addresses, or to the column addresses.
A_{10}-A_0	Address	I	X		Inputs for low-order addresses during Read and Write operations. Addresses are internally latched during a Write cycle. For the programming interface, these addresses are latched by R/C# and share the same pins as the high-order address inputs.
DQ_7-DQ_0	Data	I/O	X		To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a Write cycle. The outputs are in tri-state when OE# is high.
OE#	Output Enable	I	X		To gate the data output buffers.
WE#	Write Enable	I	X		To control the Write operations.
RES	Reserved			X	These pins must be left unconnected.
V_{DD}	Power Supply	PWR	X	X	To provide power supply (3.0-3.6V)
V_{SS}	Ground	PWR	X	X	Circuit ground (0V reference)
NC	No Connection		N/A	N/A	Unconnected pins.

T1.0 1226

1. I = Input, O = Output

Clock

The LCLK pin accepts a clock input from the host controller.

Input/Output Communications

The LAD[3:0] pins are used to serially communicate cycle information such as cycle type, cycle direction, ID selection, address, data, and sync fields.

Input Communication Frame

The LFRAME# pin is used to indicate start of a LPC bus cycle. The pin is also used to abort an LPC bus cycle in progress.

Interface Mode Select

The MODE pin is used to set the interface mode. If the mode pin is set to logic high, the device is in PP mode. If the mode pin is set low, the device is in the LPC mode. The mode selection pin must be configured prior to device operation. The mode pin is internally pulled down if the pin is left unconnected.

Reset

A V_{IL} on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization. During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, LAD[3:0], in a high impedance state. The reset signal must be held low for a minimum of time T_{RSTP}. A reset latency occurs if a reset procedure is performed during a Program or Erase operation. See Table 20 and Table 21, Reset Timing Parameters, for more information. A device reset during an active Program or Erase operation will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation.

Identification Inputs

These pins are part of a mechanism that allows multiple devices to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0] = 0; all subsequent devices should use sequential count-up strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ

General Purpose Inputs

The General Purpose Inputs (GPI[4:0]) can be used as digital inputs for the CPU to read. The GPI register holds the values on these pins. The data on the GPI pins must be stable before the start of a GPI register Read and remain stable until the Read cycle is complete. The pins must be driven low, V_{IL}, or high, V_{IH} but not left unconnected (float).

Write Protect / Top Block Lock

The Top Boot Lock (TBL#) and Write Protect (WP#) pins are provided for hardware write protection of device memory in the SST49LF040B. The TBL# pin is used to write protect 16 boot sectors (64 KByte) at the highest memory address range for the SST49LF040B. The WP# pin write protects the remaining sectors in the flash memory.

An active low signal at the TBL# pin prevents Program and Erase operations of the top boot block. When TBL# pin is held high, the hardware write protection of the top boot block is disabled. The WP# pin serves the same function for the remaining blocks of the device memory. The TBL# and WP# pins write protection functions operate independently of one another. Both TBL# and WP# pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP# pin during a Program or Erase operation could cause unpredictable results.

Row / Column Select

The R/C# pin is used to control the multiplex address inputs in Parallel Programming (PP) mode. The column addresses are mapped to the higher internal addresses (A_{18-11}) and the row addresses are mapped to the lower internal addresses (A_{10-0}).

Output Enable

The OE# pin is used to gate the output data buffers in PP mode.

Write Enable

The WE# pin is used to control the write operations in PP mode.

No Connection

These pins are not connected internally.

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DEVICE MEMORY MAP

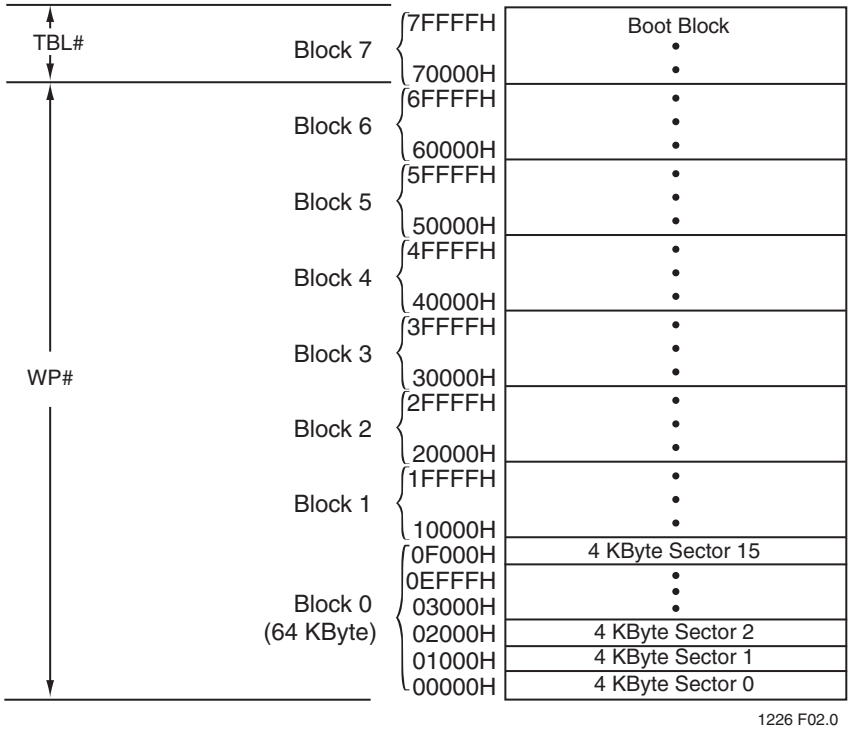

FIGURE 4: Device Memory Map

DESIGN CONSIDERATIONS

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin. If a socket is used for programming purposes, an additional 1-10 µF should be added next to each socket.

The RST# and INIT# pins must remain stable at V_{IH} for the entire duration of an Erase or Program operation. WP# must remain stable at V_{IH} for the entire duration of the Erase and Program operations for non-Boot Block sectors. To write data to the top Boot Block sectors, the TBL# pin must also remain stable at V_{IH} for the entire duration of the Erase and Program operations.

PRODUCT IDENTIFICATION

The Product Identification mode identifies the device as the SST49LF040B and manufacturer as SST.

TABLE 2: Product Identification

	Address		Data
	PP Mode	LPC Mode[1]	
Manufacturer's ID	0000H	FFBC 0000H	BFH
Device ID SST49LF040B	0001H	FFBC 0001H	50H

T2.0 1226

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins when multiple LPC memory devices are used in a system.

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MODE SELECTION

The SST49LF040B flash memory device operates in two distinct interface modes: the LPC mode and the Parallel Programming (PP) mode. The MODE (Interface Mode Select) pin is used to set the interface mode selection. If the MODE pin is set to logic high, the device is in PP mode; while if the MODE pin is set low, the device is in LPC mode. The MODE selection pin must be configured prior to device operation and must not change during operation. If the pin is not connected, by default the Mode pin is internally pulled low and the 49LF040B will be in LPC operation.

In LPC mode, communication between the Host and the 49LF040B occurs via the 4-bit I/O communication signals, LAD[3:0] and LFRAME#. The 49LF040B detects the start of an LPC cycle by reading the START field contents; a 0000b indicates the beginning of an LPC memory cycle.

In PP mode, the device is controlled via the 11 addresses, A_{10}-A_0, and 8 I/O, DQ_7-DQ_0, signals. The address inputs are multiplexed in row and column selected by control signal R/C# pin. The row addresses are mapped to the lower internal addresses (A_{10-0}), and the column addresses are mapped to the higher internal addresses (A_{18-11}). See Figure 4, Device Memory Map, for address assignments.

LPC MODE

Device Operation

The LPC mode uses a 5-signal communication interface consisting of one control line, LFRAME#, which is driven by the host to start or abort a bus cycle, and a 4-bit data bus, LAD[3:0], which is used to communicate cycle type, cycle direction, ID selection, address, data and sync fields. The device enters standby mode when LFRAME# is high and no internal operation is in progress.

The SST49LF040B supports single-byte LPC Memory Read/Write cycles as defined in Intel's Low-Pin-Count Interface Specification. The host drives LFRAME# low for one or more clock cycles to initiate an LPC cycle. The last latched value of LAD[3:0] before LFRAME# is the START value as defined in Tables 3 and 4 as well as Figures 5 and 6.

JEDEC standard SDP (Software Data Protection) Program and Erase command sequences are used to initiate LPC Memory Program and Erase operations. See Table 10 for a listing of Program and Erase commands. Chip-Erase is only available in PP mode.

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LPC Memory Read Cycle

TABLE 3: LPC Memory Read Cycle Field Definitions

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	0000	IN	LFRAME# must be active (low) for the device to respond. Only the last field latched before LFRAME# transitions high will be recognized. The START field contents (0000b) indicate an LPC Memory cycle.
2	CYCTYPE + DIR	010X	IN	Indicates the type of LPC Memory cycle. Bits 3:2 must be “01b” for memory cycle. Bit 1 indicates the type of transfer “0” for Read. Bit 0 is reserved.
3-10	ADDR	YYYY	IN	Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first.
11	TAR0	1111	IN then Float	In this clock cycle, the host drives the bus to all 1s and then floats the bus. This is the first part of the bus “turnaround cycle.”
12	TAR1	1111 (float)	Float then OUT	The SST49LF040B takes control of the bus during this cycle.
13	SYNC	0000	OUT	The SST49LF040B outputs the value 0000b indicating that it has received data.
14	DATA	ZZZZ	OUT	ZZZZ is the least-significant nibble of the data byte.
15	DATA	ZZZZ	OUT	ZZZZ is the most-significant nibble of the data byte.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF040B drives the bus to all 1s and then floats the bus. This is the first part of the bus “turn-around cycle.”
17	TAR1	1111 (float)	Float then IN	The host takes control of the bus during this cycle.

T3.0 1226

1. Field contents are valid on the rising edge of the present clock cycle.

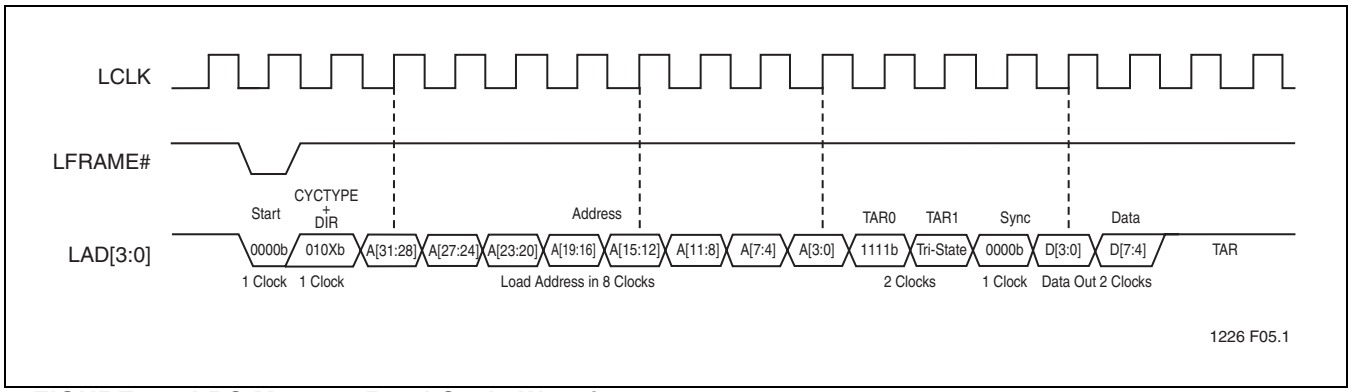

FIGURE 5: LPC Memory Read Cycle Waveform

LPC Memory Write Cycle

TABLE 4: LPC Memory Write Cycle Field Definitions

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	0000	IN	LFRAME# must be active (low) for the device to respond. Only the last field latched before LFRAME# transitions high will be recognized. The START field contents (0000b) indicate an LPC Memory cycle.
2	CYCTYPE + DIR	011X	IN	Indicates the type of LPC Memory cycle. Bits 3:2 must be “01b” for memory cycle. Bit 1 indicates the type of transfer “1” for Write. Bit 0 is reserved.
3-10	ADDR	YYYY	IN	Address Phase for Memory Cycle. LPC protocol supports a 32-bit address phase. YYYY is one nibble of the entire address. Addresses are transferred most significant nibble first.
11	DATA	ZZZZ	IN	ZZZZ is the least-significant nibble of the data byte.
12	DATA	ZZZZ	IN	ZZZZ is the most-significant nibble of the data byte.
13	TAR0	1111	IN	In this clock cycle, the host drives the bus to all '1's and then floats the bus. This is the first part of the bus “turnaround cycle.”
14	TAR1	1111 (float)	Float then OUT	The SST49LF040B takes control of the bus during this cycle.
15	SYNC	0000	OUT	The SST49LF040B outputs the values 0000, indicating that it has received data or a flash command.
16	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF040B drives the bus to all '1's and then floats the bus. This is the first part of the bus “turnaround cycle.”
17	TAR1	1111 (float)	Float then IN	Host resumes control of the bus during this cycle.

T4.0 1226

1. Field contents are valid on the rising edge of the present clock cycle.

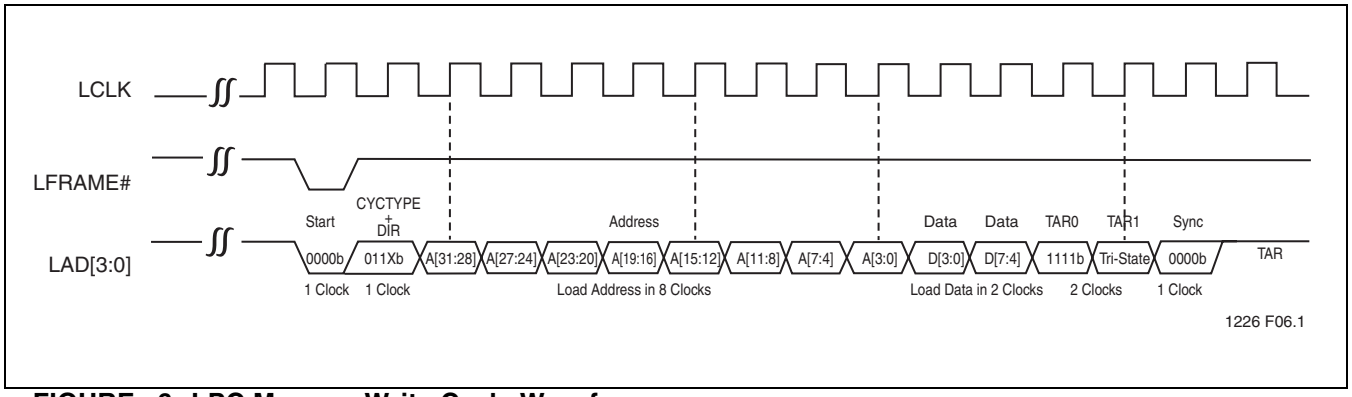

FIGURE 6: LPC Memory Write Cycle Waveform

Abort Mechanism

If LFRAME# is driven low for one or more clock cycles after the start of a bus cycle, the cycle will be terminated. The host may drive LAD[3:0] with '1111b' (ABORT nibble) to return the interface to ready mode. The ABORT only affects the current bus cycle. For a multi-cycle command sequence, such as the Erase or Program SDP commands, ABORT doesn't interrupt the entire command sequence, only the current bus cycle of the command sequence. The host can re-send the bus cycle for the aborted command and continue the SDP command sequence after the device is ready again.

Response to Invalid Fields for LPC Memory Cycle

ID mismatch: ID information is included in the address bits of every LPC Memory cycle, see Table 6. The SST49LF040B will compare the ID bits in the address field with ID[3:0]. If the ID bits in the address do not correspond to the hardware ID pins the device will ignore the cycle.

Address out of range: The address sequence is 8 fields long (32 bits). Address A_{22} has the special function of directing reads and writes to the flash core (A_{22}=1) or to the register space (A_{22}=0). The SST49LF040B will only respond to address range specified in Table 5.

Once valid START, CYCTYPE + DIR, and address range (including ID bits) are received, the SST49LF040B will always complete the bus cycle. However, if the device is busy performing a flash Erase or Program operation, no new internal Write command (memory Write or register Write) will be executed. As long as the states of LAD[3:0] and LFRAME# are known, the response of the SST49LF040B to signals received during the LPC cycle should be predictable.

TABLE 5: LPC Memory Address Decoding Range

ID Strapping	Device Access	Address Range	Memory Size
Device #0 - 7	Memory Access	FFFF FFFFH : FFC0 0000H	4 MByte
	Register Access	FFBF FFFFH : FF80 0000H	4 MByte
Device #8 - 15	Memory Access	FF7F FFFFH : FF40 0000H	4 MByte
	Register Access	FF3F FFFFH : FF00 0000H	4 MByte
Device #0[1]	Memory Access	000F FFFFH : 000E 0000H	128 KByte

T5.0 1226

1. For device #0 (Boot Device), SST49LF040B decodes the physical addresses of the top 2 blocks (including Boot Block) both at system memory ranges FFFF FFFFH to FFFE 0000H and 000F FFFFH to 000E 0000H.

TABLE 6: LPC Memory Address bits definition

A_{31}: A_{24}[1]	A_{23}	A_{22}	A_{21}: A_{19}	A_{18}:A_0
1111 1111b or 0000 0000b	ID[3][2]	1 = Memory Access 0 = Register access	ID[2:0][2]	Device Memory address

T6.0 1226

1. For SST49LF040B, the top 16 MByte address range FFFF FFFFH to FF00 0000H and the bottom 128 KByte memory access address 000F FFFFH to 000E 0000H are decoded.
2. See Table 7 for multiple device selection configuration.

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Multiple Device Selection

Multiple LPC Flash devices may be strapped to increase memory densities in a system. The four ID strapping pins, ID[3:0], allow up to 16 devices to be attached to the same bus by using different ID strapping in a system. Equal density must be used with multiple devices. BIOS support, bus loading or the attaching bridge may limit this number. The maximum “window” of the LPC array visible at one time is 16 MByte.

For applications that boot from the top address of the 4 GByte system memory map, the ID strapping is sequentially incremented downward.

With hardware strapping, ID bits in the address field is included in every LPC address memory cycle. The ID select bits [A23, A21: A19] are used to select the device with proper IDs. The ID strapping bits in the address field will be decoded depending on where the device is mapped on the 4 GByte system memory map. See Table 7 for ID address bits decoding. The device will compare these bits with ID[3:0]’s strapping values. If there is a mismatch, the device will ignore the remainder of the cycle.

TABLE 7: LPC Memory Multiple Device Selection Configuration

Device #	ID[3:0]	Address Range[1]
0 (Boot device)	0000	1111
1	0001	1110
2	0010	1101
3	0011	1100
4	0100	1011
5	0101	1010
6	0110	1001
7	0111	1000
8	1000	0111
9	1001	0110
10	1010	0101
11	1011	0100
12	1100	0011
13	1101	0010
14	1110	0001
15	1111	0000

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1. A_{23}, A_{21}:A_{19}

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Write Operation Status Detection

The SST49LF040B device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling, D[7], and Toggle Bit, D[6]. The End-of-Write detection mode is incorporated into the LPC Memory Read cycles. The actual completion of the nonvolatile write is asynchronous with the system. Therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either D[7] or D[6]. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Data# Polling

When the SST49LF040B device is in the internal Program operation, any attempt to read D[7] will produce the complement of the true data. Once the Program operation is completed, D[7] will produce true data. Note that even though D[7] may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data will appear on the entire data bus in subsequent successive Read cycles after an interval of 1 µs. During an internal Erase operation, any attempt to read D[7] will produce a '0'. Once the internal Erase operation is completed, D[7] will produce a '1'. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit

During the internal Program or Erase operation, any consecutive attempts to read D[6] will produce alternating 0s and 1s, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. Note that even though D[6] may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data will appear on the entire data bus in subsequent successive Read cycles after an interval of 1 µs. Proper status will not be given using Toggle Bit if the address is in the invalid range.

Registers

There are three types of registers available on the SST49LF040B, the General Purpose Inputs register, Block Locking registers, and the JEDEC ID registers. These registers appear at their respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read or write any register during an internal Write operation will be ignored.

General Purpose Inputs Register

The GPI_REG (General Purpose Inputs Register) passes the state of GPI[4:0] to the outputs. It is recommended that the GPI[4:0] pins are in the desired state before LFRAME# is brought low for the beginning of the bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. The GPI register for the boot device appears at FFBC0100H in the 4 GByte system memory map, and will appear elsewhere if the device is not the boot device. The register is not available to be read when the device is in Erase/Program operation.

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Block Locking Registers

SST49LF040B provides software controlled lock protection through a set of Block Locking registers. The Block Locking registers are Read/Write registers and are accessible through standard addressable memory locations specified in Tables 8 and 9 for boot device. These registers will appear elsewhere if the device is not the boot device. Unused register locations will read as 00H.

Write Lock: The Write-Lock bit, bit 0, controls the lock state. The default Write status of all blocks after power up is write locked. When bit 0 of the Block Locking register is set, Program and Erase operations for the corresponding block are prevented. Clearing the Write-Lock bit will unprotect the block. The Write-Lock bit must be cleared prior to starting a Program or Erase operation since it is sampled at the beginning of the operation. The Write-Lock bit functions in conjunction with the hardware Write Lock pin TBL# for the top Boot Block. When TBL# is low, it overrides the software locking scheme. The top Boot Block Locking register does not indicate the state of the TBL# pin. The Write-Lock bit functions in conjunction with the hardware WP# pin for blocks 0 to 6. When WP# is low, it overrides the software locking scheme. The Block Locking registers do not indicate the state of the WP# pin.

Lock Down: The Lock-Down bit, bit 1, controls the Block Locking registers. The default Lock Down status of all blocks upon power-up is not locked down. Once the Lock-Down bit is set, any future attempted changes to that Block Locking register will be ignored. The Lock-Down bit is only cleared upon a device reset with RST# or INIT# or power down. Current Lock Down status of a particular block can be determined by reading the corresponding Lock-Down bit.

JEDEC ID Registers

The JEDEC ID registers provide access to the manufacturer and device ID information with a single Read cycle. The JEDEC ID registers for the boot device appear at FFBC0000H and FFBC0001H in the 4 GByte system memory map, and will appear elsewhere if the device is not the boot device. Registers are not available for read when the device is in Erase/Program operation. Refer to Table 2 for product identification information.

TABLE 8: Block Locking Registers[1]

Register	Block Size	Protected Memory Address Range	Memory Map Register Address
T_BLOCK_LK	64K	07FFFFH - 070000H	FFBF0002H
T_MINUS01_LK	64K	06FFFFH - 060000H	FFBE0002H
T_MINUS02_LK	64K	05FFFFH - 050000H	FFBD0002H
T_MINUS03_LK	64K	04FFFFH - 040000H	FFBC0002H
T_MINUS04_LK	64K	03FFFFH - 030000H	FFBB0002H
T_MINUS05_LK	64K	02FFFFH - 020000H	FFBA0002H
T_MINUS06_LK	64K	01FFFFH - 010000H	FFB90002H
T_MINUS07_LK	64K	00FFFFH - 000000H	FFB80002H

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1. Default value at power up is 01H

TABLE 9: Block Locking Register Bits

Reserved Bit [7..2]	Lock-Down Bit [1]	Write-Lock Bit [0]	Lock Status
000000	0	0	Full Access
000000	0	1	Write Locked (Default State at Power-Up)
000000	1	0	Locked Open (Full Access Locked Down)
000000	1	1	Write Locked Down

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PARALLEL PROGRAMMING MODE

Device Operation

Commands are used to initiate the memory operation functions of the device. The data portion of the software command sequence is latched on the rising edge of WE#. During the software command sequence the row address is latched on the falling edge of R/C# and the column address is latched on the rising edge of R/C#.

Read

The Read operation of the SST49LF040B device is controlled by OE#. OE# is the output control and is used to gate data from the output pins. Refer to the Read cycle timing diagram, Figure 12, for further details.

Reset

A V_{IL} on RST# pin initiates a device reset.

Byte-Program Operation

The SST49LF040B device is programmed on a byte-by-byte basis. Before programming, one must ensure that the byte that is being programmed is fully erased. The Byte-Program operation is initiated by executing a four-byte command load sequence for Software Data Protection with address (PA) and data in the last bus cycle. During the Byte-Program operation, the row address (A_{10}-A_0) is latched on the falling edge of R/C# and the column Address (A_{21}-A_{11}) is latched on the rising edge of R/C#. The data bus is latched on the rising edge of WE#. The Program operation, once initiated, will be completed, within 20 µs. See Figure 16 for timing waveforms. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands written during the internal Program operation will be ignored.

Sector-Erase Operation

The Sector-Erase operation allows the system to erase the device on a sector-by-sector basis. The sector architecture is based on uniform sector size of 4 KByte. The Sector-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 17 for Sector-Erase timing waveforms. Any commands written during the Sector-Erase operation will be ignored.

Block-Erase Operation

The Block-Erase operation allows the system to erase the device in any of the 8 uniform 64 KByte blocks for the SST49LF040B The Block-Erase operation is initiated by executing a six-byte command load sequence for Software Data Protection with Block-Erase command (50H) and block address (BA) in the last bus cycle. The internal Block-Erase operation begins after the sixth WE# pulse. The End-of-Erase can be determined using either Data# Polling or Toggle Bit methods. See Figure 18 for timing waveforms. Any commands written during the Block- Erase operation will be ignored.

Chip-Erase Operation

The SST49LF040B device provides a Chip-Erase operation only in PP mode, which allows the user to erase the entire memory array to the '1's state. This is useful when the entire device must be quickly erased. The Chip-Erase operation is initiated by executing a six- byte Software Data Protection command sequence with Chip- Erase command (10H) with address 5555H in the last bus cycle. The internal Erase operation begins with the rising edge of the sixth WE#. During the internal Erase operation, the only valid reads are Toggle Bit or Data# Polling. See Table 11 for the command sequence, Figure 19 for timing diagram. Any commands written during the Chip-Erase operation will be ignored.

Write Operation Status Detection

The SST49LF040B device provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE# which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, the device has completed the Write cycle, otherwise the rejection is valid.

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TABLE 10: Operation Modes Selection (PP Mode)

Mode	RST#	OE#	WE#	DQ	Address
Read	V_{IH}	V_{IL}	V_{IH}	D_{OUT}	A_{IN}
Program	V_{IH}	V_{IH}	V_{IL}	D_{IN}	A_{IN}
Erase	V_{IH}	V_{IH}	V_{IL}	X[1]	Sector or Block address, XXH for Chip-Erase
Reset	V_{IL}	X	X	High Z	X
Write Inhibit	V_{IH}	V_{IL}	V_{IH}	High Z/D_{OUT}	X
Product Identification	V_{IH}	V_{IL}	V_{IH}	Manufacturer's ID (BFH) Device ID (50H)	A_{18} - A_1 = V_{IL}, A_0 = V_{IL} A_{18} - A_1 = V_{IL}, A_0 = V_{IH}

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1. X can be V_{IL} or V_{IH}, but no other value.

Data# Polling (DQ_7)

When the SST49LF040B device is in the internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. Note that even though DQ_7 may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid. Valid data will appear on the entire data bus in subsequent successive Read cycles after an interval of 1 µs. During an internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. Data# Polling is valid after the rising edge of the fourth WE# pulse for the Program operation. For Sector-Erase, Block-Erase, or Chip-Erase, the Data# Polling is valid after the rising edge of the sixth WE# pulse. See Figure 14 for Data# Polling timing diagram. Proper status will not be given using Data# Polling if the address is in the invalid range.

Toggle Bit (DQ_6)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating '0's and '1's, i.e., toggling between 0 and 1. When the internal Program or Erase operation is completed, the toggling will stop. The device is then ready for the next operation. The Toggle Bit is valid after the rising edge of the fourth WE# pulse for Program operation. For Sector-Erase, Block-Erase or Chip-Erase, the Toggle Bit is valid after the rising edge of the sixth WE# pulse. See Figure 15 for Toggle Bit timing diagram.

Data Protection (PP Mode)

The SST49LF040B device provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST49LF040B provides the JEDEC approved Software Data Protection scheme for all data alteration operation, i.e., Program and Erase. Any Program operation requires the inclusion of a series of three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power down. Any Erase operation requires the inclusion of a five-byte load sequence.

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SOFTWARE COMMAND SEQUENCE

TABLE 11: Software Command Sequence

Command Sequence	1st[1] Cycle		2nd[1] Cycle		3rd[1] Cycle		4th[1] Cycle		5th[1] Cycle		6th[1] Cycle	
	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data	Addr[2]	Data
Byte-Program	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	A0H	PA[3]	Data				
Sector-Erase	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	SA_X[4]	30H
Block-Erase	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	BA_X[5]	50H
Chip-Erase[6]	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	80H	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	10H
Software ID Entry[7,8]	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	90H	Read ID					
Software ID Exit[9]	XXXX XXXXH	F0H										
Software ID Exit[9]	YYYY 5555H	AAH	YYYY 2AAAH	55H	YYYY 5555H	F0H						

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1. LPC mode use consecutive Write cycles to complete a command sequence; PP mode use consecutive bus cycles to complete a command sequence.
2. YYYY = A[31:16]. In LPC mode, during SDP command sequence, YYYY must be within valid memory address range, see Address out of range: section for details. In PP mode, YYYY can be V_{IL} or V_{IH}, but no other value.
3. PA = Program Byte address
4. SA_X for Sector-Erase Address
5. BA_X for Block-Erase Address
6. Chip-Erase is supported in PP mode only
7. SST Manufacturer's ID = BFH, is read with A_{18}-A_0 = 0.
   With A_{18}-A_1 = 0; 49LF040B Device ID = 50H, is read with A_0 = 1.
8. The device does not remain in Software Product ID mode if powered down.
9. Both Software ID Exit operations are equivalent

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ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the LPC interface signals (LA0[3:0], LFRAME, LCLCK and RST#) are defined in Section 4.2.2.4 of the PCI local bus specification, Rev. 2.1. Refer to Table 12 for the DC voltage and current specifications. Refer to Tables 16 through 22 for the AC timing specifications for Clock, Read, Write, and Reset operations.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential[1] . . . . . -2.0V to V_{DD}+2.0V
Package Power Dissipation Capability (T_A=25°C) 1.0W
Surface Mount Solder Reflow Temperature[2] . . . . . 260°C for 10 seconds
Output Short Circuit Current[3]. . . . . 50 mA

1. Do not violate processor or chipset limitations on the INIT# pin
2. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
3. Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC Conditions of Test[1]

Input Rise/Fall Time . . . . . 3 ns
Output Load . . . . . C_L = 30 pF
See Figures 22 and 23

1. LPC interface signals use PCI load test condition

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DC Characteristics

TABLE 12: DC Operating Characteristics (All Interfaces)

Symbol	Parameter	Limits Min	Limits Max	Limits Units	Test Conditions
I_{DD}[1]	Active V_{DD} Current				LCLK (LPC mode) and Address Input (PP mode)=V_{ILT}/V_{IHT} at f=33 MHz (LPC mode) or $1/_{TRC\ min}$ (PP mode) All other inputs=V_{IL} or V_{IH}
	Read		12	mA	All outputs = open, V_{DD}=V_{DD} Max
	Write[2]		30	mA	See Note 2
I_{SB}	Standby V_{DD} Current (LPC Interface)		100	µA	LCLK (LPC mode) and Address Input (PP mode)=V_{ILT}/V_{IHT} at f=33 MHz (LPC mode) or $1/_{TRC\ min}$ (PP mode) LFRAME#=0.9 V_{DD}, f=33 MHz, CE#=0.9 V_{DD}, V_{DD}=V_{DD} Max, All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_{RY}[3]	Input Current for Mode and ID[3:0] pins		10	mA	LCLK (LPC mode) and Address Input (PP mode)=V_{ILT}/V_{IHT} at f=33 MHz (LPC mode) or $1/_{TRC\ min}$ (PP mode) LFRAME#=V_{IL}, f=33 MHz, V_{DD}=V_{DD} Max All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_I	Input Leakage Current for Mode and ID[3:0] pins		200	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IHI}	INIT# Input High Voltage	1.1	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{ILI}	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD}=V_{DD} Min
V_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.5 V_{DD}	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.1 V_{DD}	V	
V_{OH}	Output High Voltage	0.9 V_{DD}		V	

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1. I_{DD} active while a Read or Write (Program or Erase) operation is in progress.
2. For PP mode: OE# = WE# = V_{IH}; For LPC mode: f = $1/T_{RC}$ min, LFRAME# = V_{IH}.
3. The device is in Ready mode when no activity is on the LPC bus.

TABLE 13: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 14: Pin Capacitance (V_{DD}=3.3V, T_A=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$=0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN}=0V	12 pF

T14.0 1226

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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TABLE 15: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T15.0 1226

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 16: Clock Timing Parameters (LPC Mode)

Symbol	Parameter	Min	Max	Units
T_{CYC}	LCLK Cycle Time	30		ns
T_{HIGH}	LCLK High Time	11		ns
T_{LOW}	LCLK Low Time	11		ns
-	LCLK Slew Rate (peak-to-peak)	1	4	V/ns
-	RST# or INIT# Slew Rate	50		mV/ns

T16.0 1226

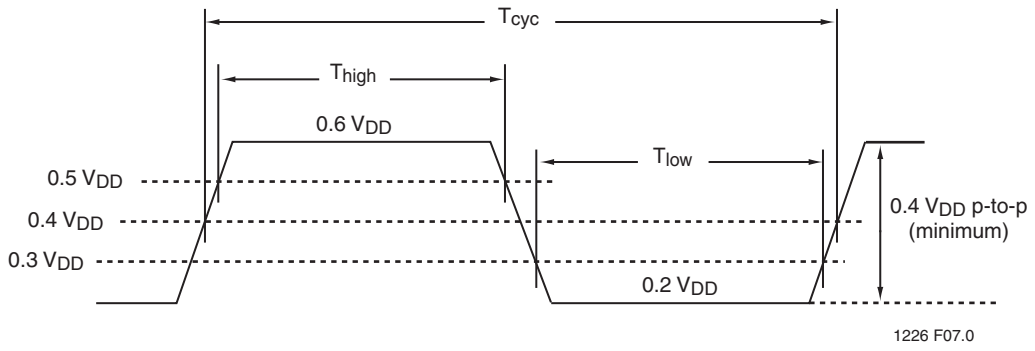

FIGURE 7: LCLK Waveform (LPC Mode)

AC Characteristics (LPC Mode)

TABLE 17: Read/Write Cycle Timing Parameters, V_{DD}=3.0-3.6V (LPC Mode)

Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Data Set Up Time to Clock Rising	7		ns
T_{DH}	Clock Rising to Data Hold Time	0		ns
T_{VAL}[1]	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{ON}	Clock Rising to Active (Float to Active Delay)	2		ns
T_{OFF}	Clock Rising to Inactive (Active to Float Delay)		28	ns

T17.0 1226

1. Minimum and maximum times have different loads. See PCI spec

TABLE 18: AC Input/Output Specifications (LPC Mode)

Symbol	Parameter	Min	Max	Units	Conditions
I_{OH}(AC)	Switching Current High	-12 V_{DD}		mA	$0 < V_{OUT} \leq 0.3V_{DD}$
		-17.1(V_{DD}-V_{OUT})		mA	$0.3V_{DD} < V_{OUT} < 0.9V_{DD}$
			Equation C[1]		$0.7V_{DD} < V_{OUT} < V_{DD}$
	(Test Point)		-32 V_{DD}	mA	$V_{OUT} = 0.7V_{DD}$
I_{OL}(AC)	Switching Current Low	16 V_{DD}	Equation D[1]	mA	$V_{DD} > V_{OUT} \geq 0.6V_{DD}$
		26.7 V_{OUT}		mA	$0.6V_{DD} > V_{OUT} > 0.1V_{DD}$
					$0.18V_{DD} > V_{OUT} > 0$
	(Test Point)		38 V_{DD}	mA	$V_{OUT} = 0.18V_{DD}$
I_{CL}	Low Clamp Current	-25+(V_{IN}+1)/0.015		mA	$-3 < V_{IN} \leq -1$
I_{CH}	High Clamp Current	25+(V_{IN}-V_{DD}-1)/0.015		mA	$V_{DD}+4 > V_{IN} \geq V_{DD}+1$
slewr	Output Rise Slew Rate	1	4	V/ns	$0.2V_{DD}$-$0.6V_{DD}$ load
slewf	Output Fall Slew Rate	1	4	V/ns	$0.6V_{DD}$-$0.2V_{DD}$ load

T18.0 1226

1. See PCI spec.

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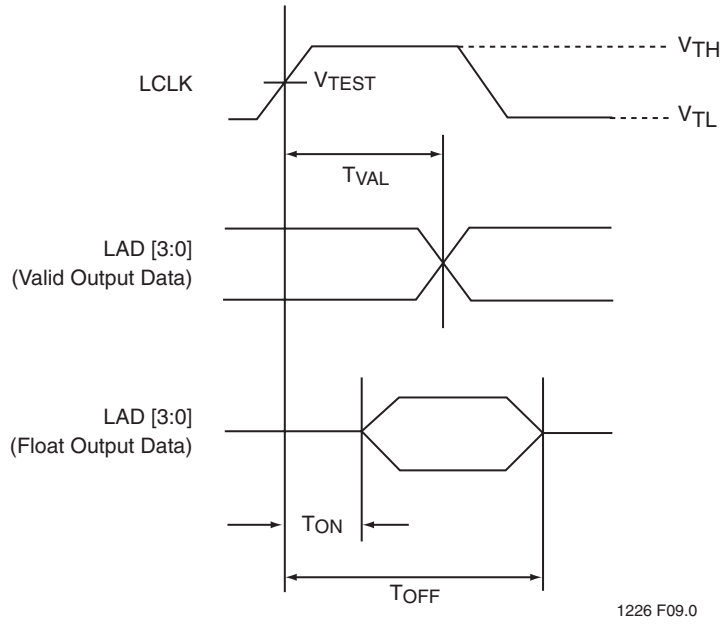

FIGURE 8: Output Timing Parameters (LPC Mode)

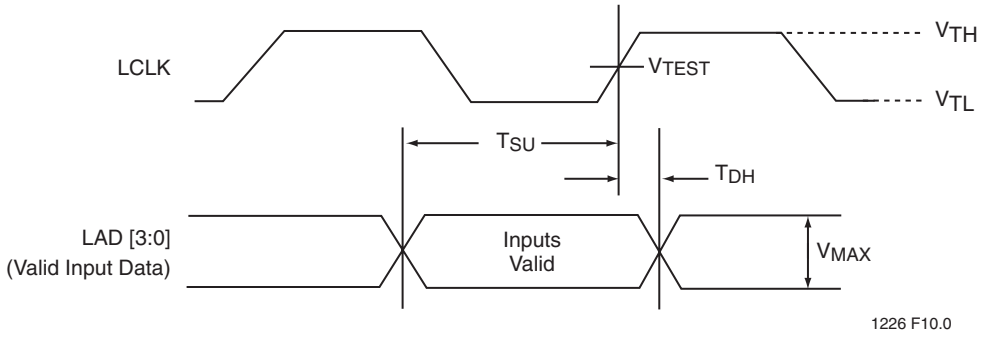

FIGURE 9: Input Timing Parameters (LPC Mode)

TABLE 19: Interface Measurement Condition Parameters (LPC Mode)

Symbol	Value	Units
V_{TH}[1]	0.6 V_{DD}	V
V_{TL}[1]	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}[1]	0.4 V_{DD}	V
Input Signal Edge Rate	1	V/ns

T19.0 1226

1. The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive than this. V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.

TABLE 20: Reset Timing Parameters, V_{DD}=3.0-3.6V (LPC Mode)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset High	100		µs
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to LFRAME# Low	5		LCLK cycles
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs

T20.0 1226

1. There will be a latency due to T_{RSTE} if a reset procedure is performed during a Program or Erase operation,

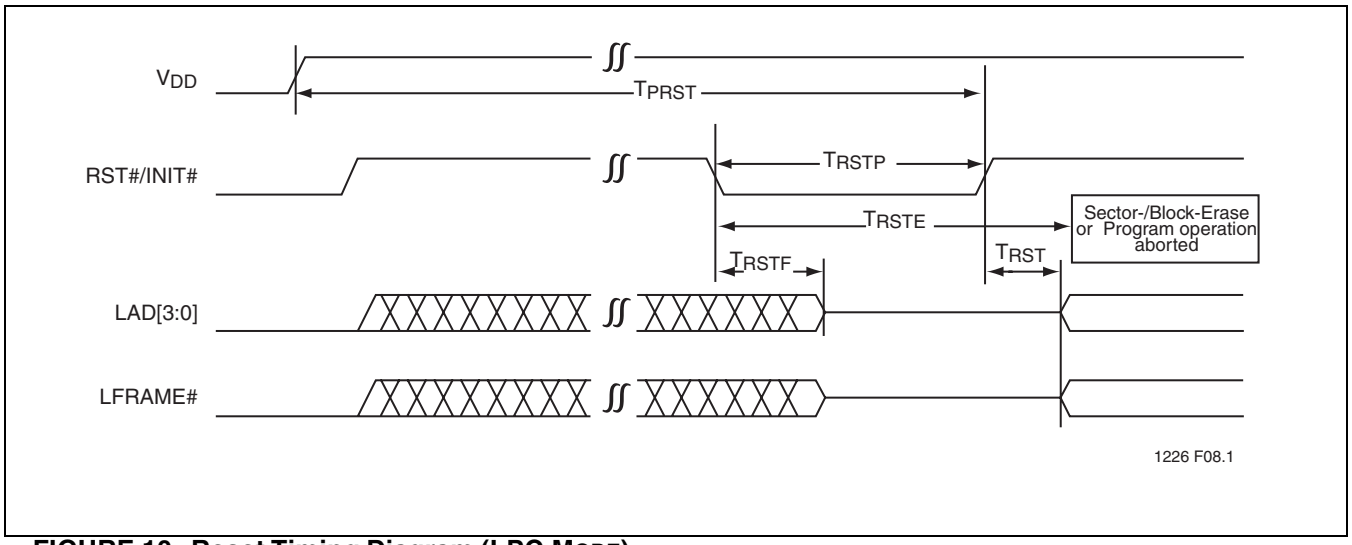

FIGURE 10: Reset Timing Diagram (LPC MODE)

TABLE 21: Reset Timing Parameters, V_{DD}=3.0-3.6V (PP Mode)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset Low	1		ms
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to Row Address Setup	1		µs
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs
T_{RSTC}	RST# Low to reset during Chip-Erase		50	µs

T21.0 1226

1. There will be a reset latency of T_{RSTE} or T_{RSTC} if a reset procedure is performed during a programming or erase operational.

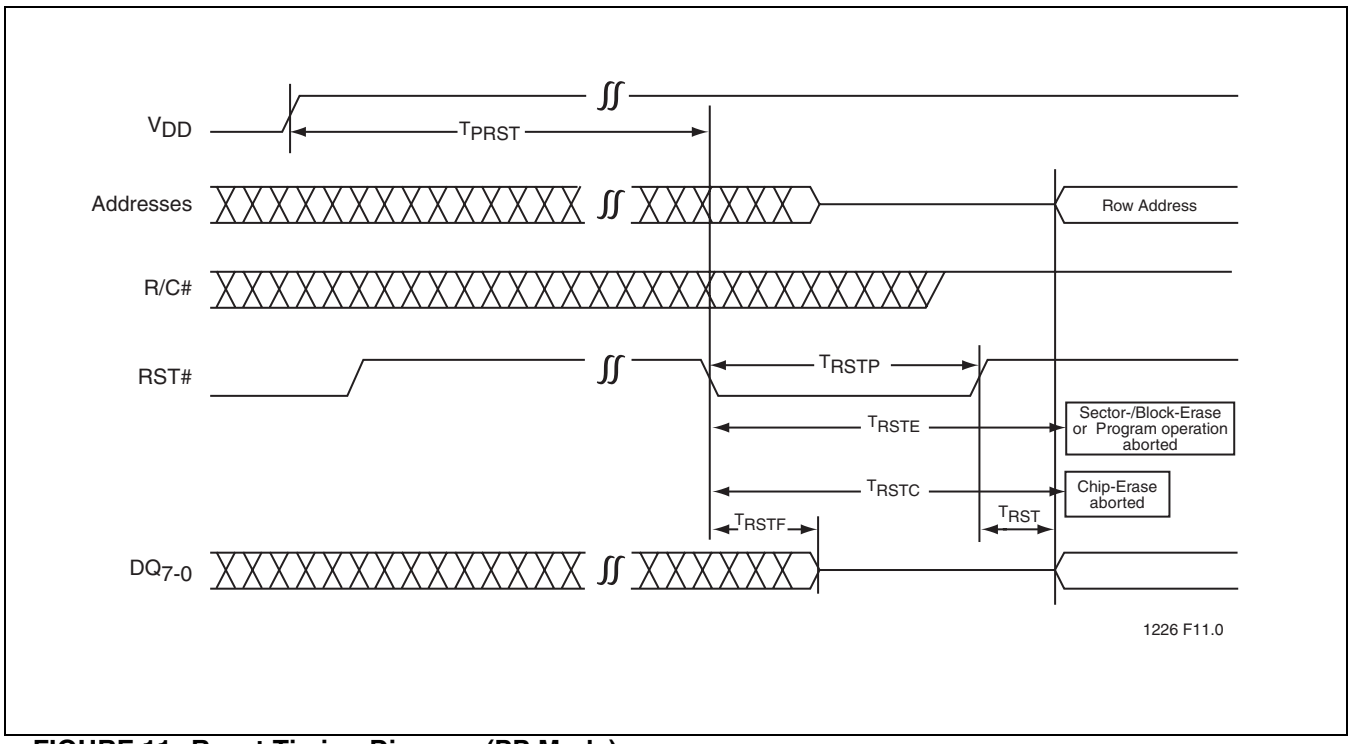

FIGURE 11: Reset Timing Diagram (PP Mode)

AC Characteristics (PP Mode)

TABLE 22: Read Cycle Timing Parameters, V_{DD}=3.0-3.6V (PP Mode)

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	270		ns
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Set-up Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{AA}	Address Access Time		120	ns
T_{OE}	Output Enable Access Time		60	ns
T_{OLZ}	OE# Low to Active Output	0		ns
T_{OHZ}	OE# High to High-Z Output		35	ns
T_{OH}	Output Hold from Address Change	0		ns

T22.0 1226

TABLE 23: Program/Erase Cycle Timing Parameters, V_{DD}=3.0-3.6V (PP Mode)

Symbol	Parameter	Min	Max	Units
T_{RST}	RST# High to Row Address Setup	1		µs
T_{AS}	R/C# Address Setup Time	45		ns
T_{AH}	R/C# Address Hold Time	45		ns
T_{CWH}	R/C# to Write Enable High Time	50		ns
T_{OES}	OE# High Setup Time	20		ns
T_{OEH}	OE# High Hold Time	20		ns
T_{OEP}	OE# to Data# Polling Delay		60	ns
T_{OET}	OE# to Toggle Bit Delay		60	ns
T_{WP}	WE# Pulse Width	100		ns
T_{WPH}	WE# Pulse Width High	100		ns
T_{DS}	Data Setup Time	50		ns
T_{DH}	Data Hold Time	5		ns
T_{IDA}	Software ID Access and Exit Time		150	ns
T_{BP}	Byte Programming Time		20	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{SCE}	Chip-Erase Time		100	ms

T23.0 1226

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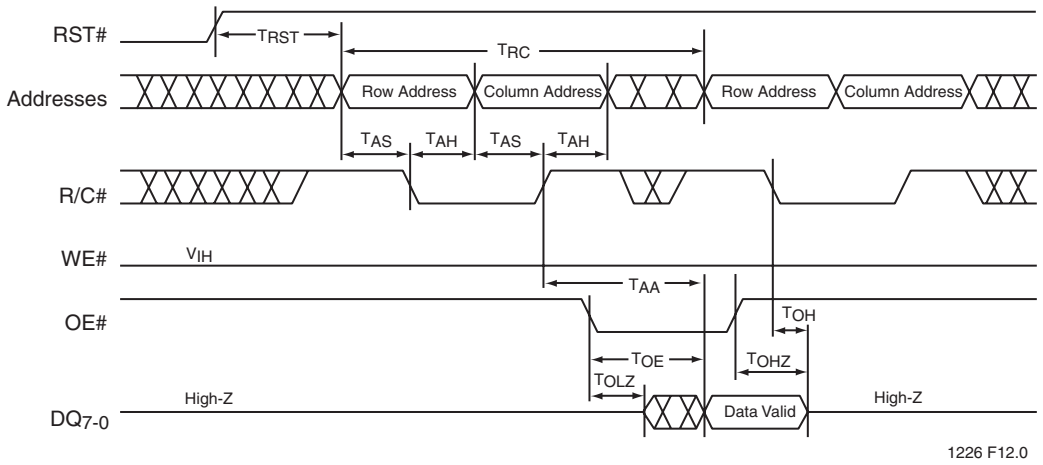


FIGURE 12: Read Cycle Timing Diagram (PP Mode)

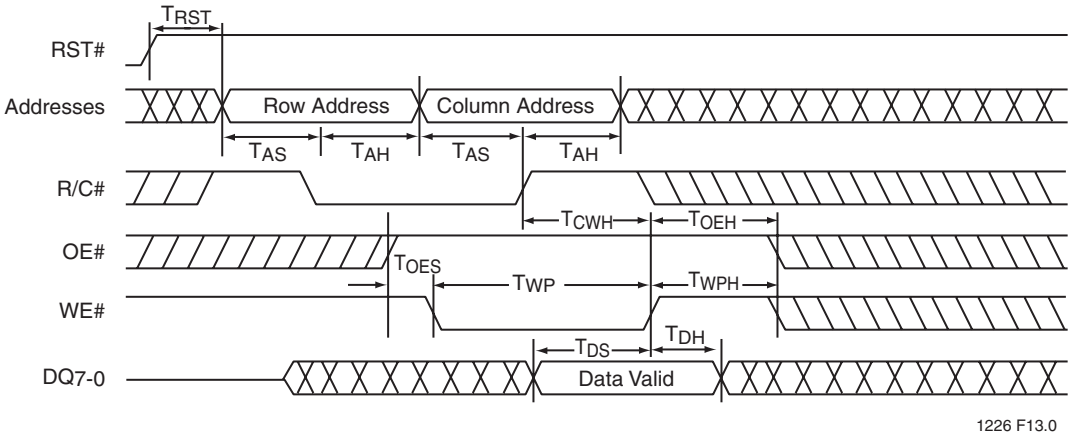


FIGURE 13: Write Cycle Timing Diagram (PP Mode)

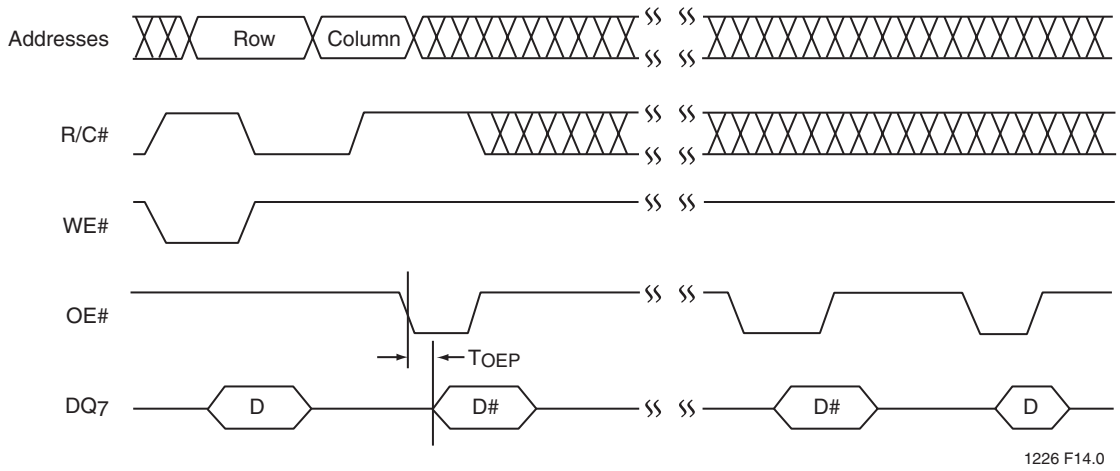


FIGURE 14: Data# Polling Timing Diagram (PP Mode)

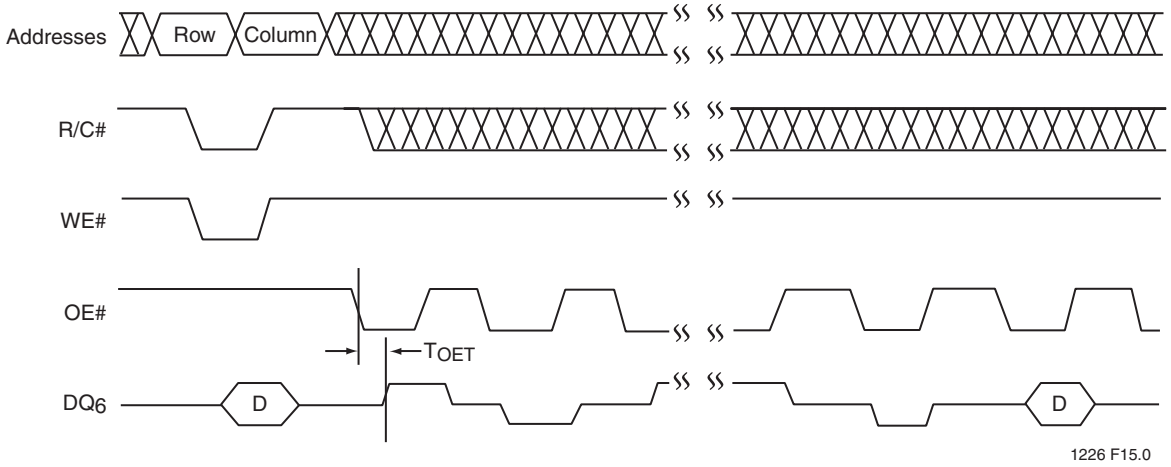


FIGURE 15: Toggle Bit Timing Diagram (PP Mode)

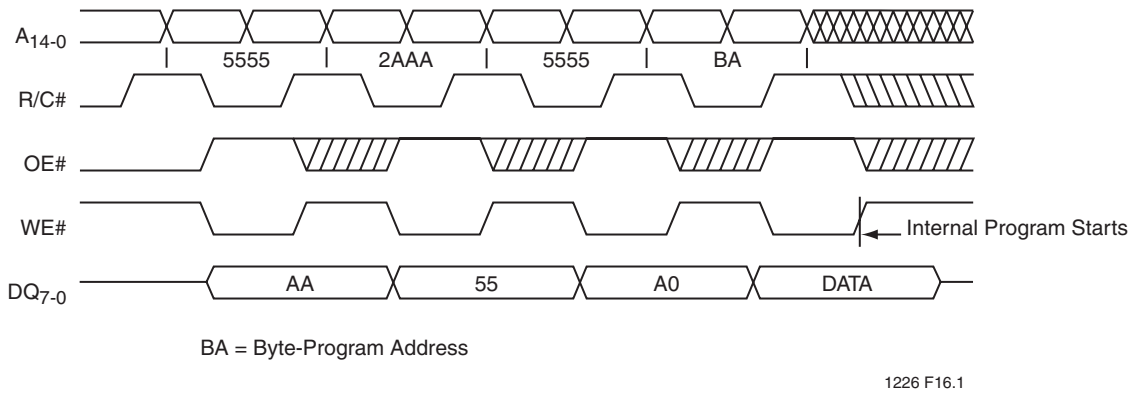


FIGURE 16: Byte-Program Timing Diagram (PP Mode)

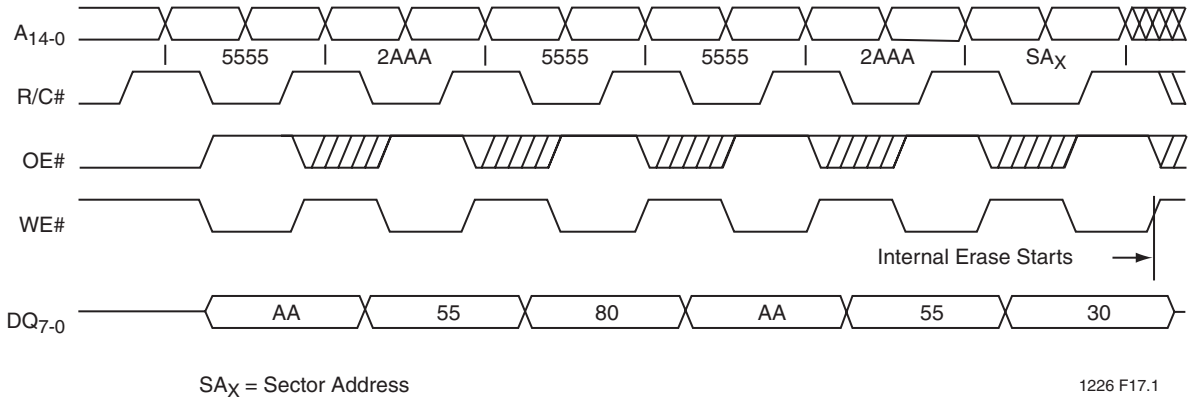


FIGURE 17: Sector-Erase Timing Diagram (PP Mode)

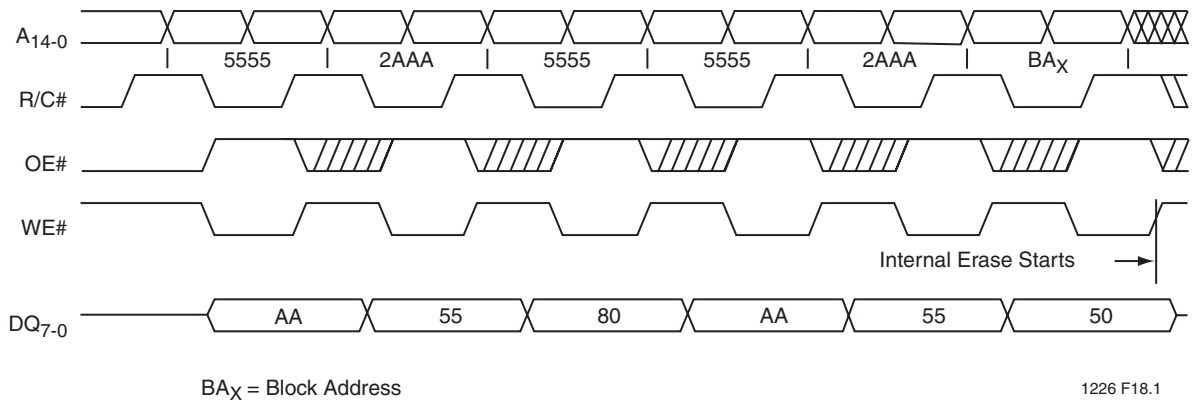


FIGURE 18: Block-Erase Timing Diagram (PP Mode)

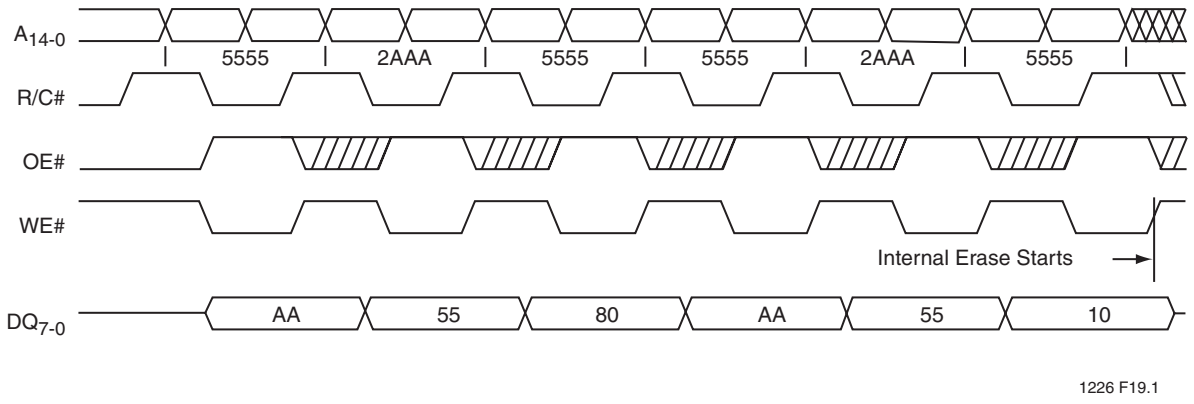


FIGURE 19: Chip-Erase Timing Diagram (PP Mode)

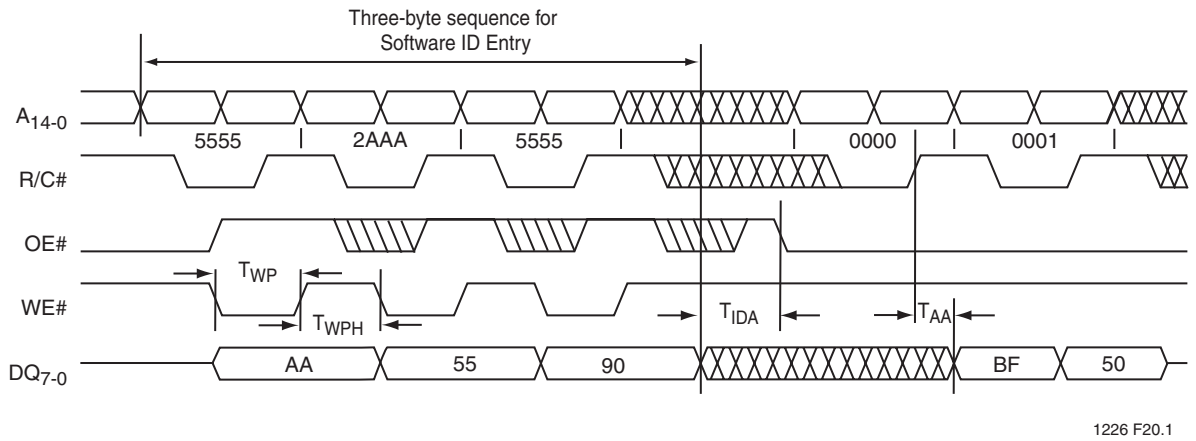


FIGURE 20: Software ID Entry and Read (PP Mode)

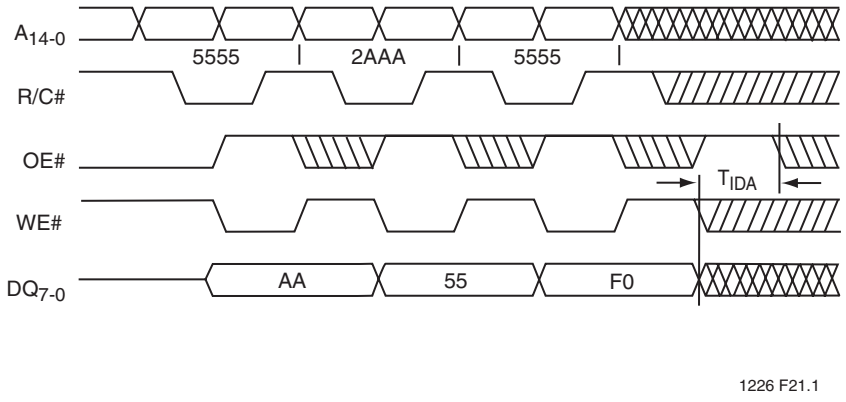
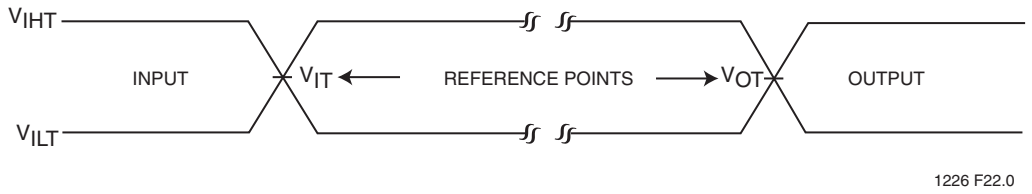


FIGURE 21: Software ID Exit (PP Mode)



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 22: AC Input/Output Reference Waveforms

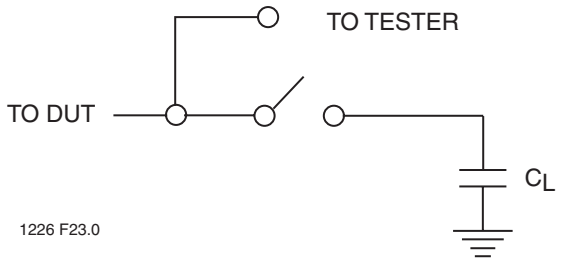


FIGURE 23: A Test Load Example

PRODUCT ORDERING INFORMATION

Device	Speed	Suffix1	Suffix2
SST49LF040B -	XXX -	XX -	XXX

Environmental Attribute
E[1] = non-Pb

Package Modifier
H = 32 leads

Package Type
N = PLCC
W = TSOP (type 1, die up, 8mm x 14mm)

Operating Temperature
C = Commercial = 0°C to +85°C

Minimum Endurance
4 = 10,000 cycles

Serial Access Clock Frequency
33 = 33 MHz

Device Density
040 = 4 Mbit

Voltage Range
L = 3.0-3.6V

Product Series
49 = LPC Firmware Memories

1. Environmental suffix “E” denotes non-Pb solder. SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST49LF040B

SST49LF040B-33-4C-WHE SST49LF040B-33-4C-NHE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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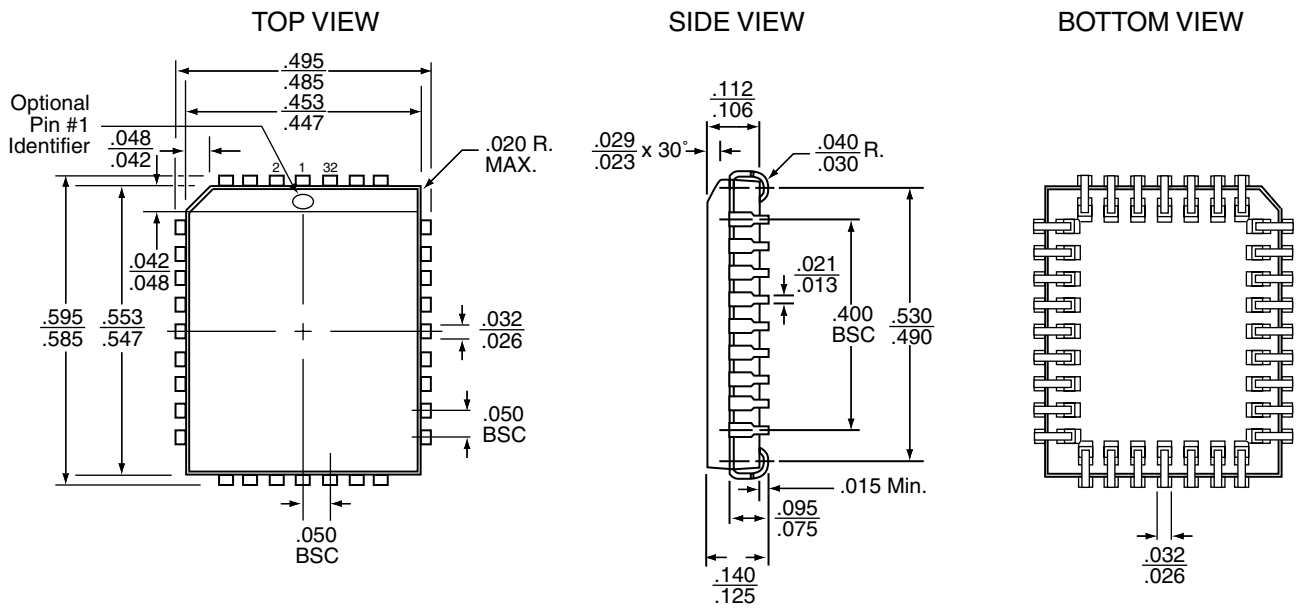
EOL Data Sheet

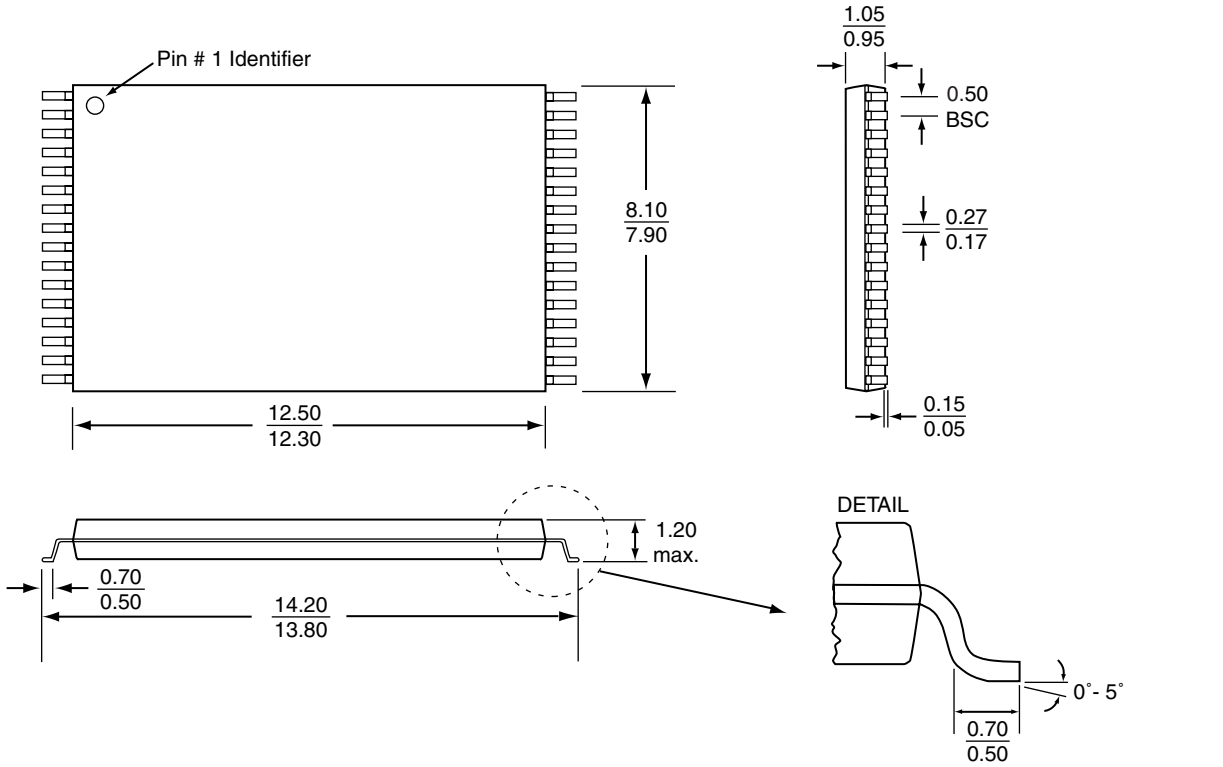
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32-plcc-NH-3

FIGURE 24: 32-lead Plastic Lead Chip Carrier (PLCC)
SST Package Code: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

FIGURE 25: 32-lead Thin Small Outline Package (TSOP) 8mm x 14mm SST Package Code: WH

EOL Data Sheet

TABLE 24: Revision History

Number	Description	Date
00	• Initial release	Dec 2002
01	• Clarified valid memory address range for LPC memory cycle	Jan 2003
02	• Removed the CE# signal from Figures 5 and 6 • Added 32-TSOP (WH/WHE) package and MPNs • Removed 40-TSOP (EI/EIE) package and MPNs • Clarified the solder temperature profile under “Absolute Maximum Stress Ratings” on page 21 • Added RoHS compliance information on page 1 and in the “Product Ordering Information” on page 35 • Removed leaded part numbers • Removed reference to Intel Specification 1.1 • Updated Figure 3 on page 7 • Removed System Memory Mapping. • Updated Table 7 on page 15. • Updated Table 8 on page 17.	Jan 2006
03	• Updated Table 3 on page 12.	May 2006
04	• End-of-Life Data Sheet for SST49LF040B	Jul 2007

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