SST89C5x to SST89E/V5xRD and SST89E/V5xRD2 Code Conversion Guide

Application Note
December 2004

1.0 INTRODUCTION

This document provides guidelines to convert existing firmware code on the SST89C5x to run on the SST89E/V54RD, SST89E/V54RD2, SST89E/V58RD, and SST89E/V58RD2 devices. New features unique to the SST89E/V5xRD and SST89E/V5xRD2 that do not pertain to the SST89C5x are not mentioned in this document. Additionally, for conciseness, the term SST89x5xRDx will be used throughout this document when referring to the following: SST89E/V54RD, SST89E/V54RD2, SST89E/V58RD, or SST89E/V58RD2.

2.0 PROGRAM MEMORY ORGANIZATION AND IN-APPLICATION PROGRAMMING

If the SST89x54RDx is used with external code memory, special note should be taken. The external code memory is not accessible in internal mode (EA# = 1). See Figure 2-1 below.

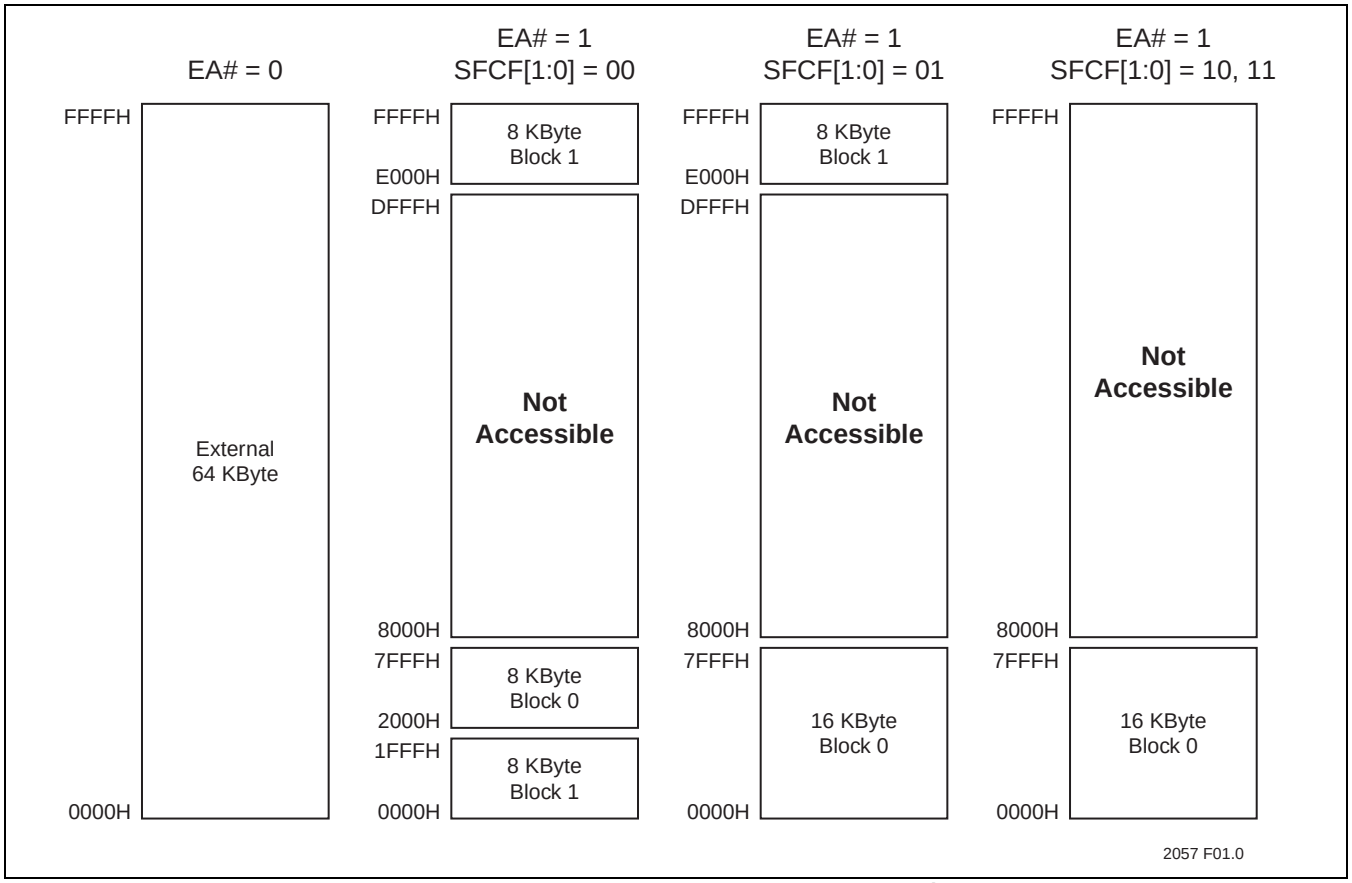

FIGURE 2-1: PROGRAM MEMORY ORGANIZATION FOR 16 KBYTE SST89E/V54RDX

Application Note

The following differences should be considered for the flash blocks and IAP:

1. The organization, size and default arrangements of the two flash blocks are different.

TABLE 2-1: FLASH MEMORY DIFFERENCES BY MCU MODEL

	SST89x58RDx	SST89x54RDx	SST89C58	SST89C54
Block 1 Size	8K		4K	
Block 0 Size	32K	16K	32K	16K
Default Starting Address: Block 1	E000H	E000H	F000H	
Default Starting Address: Block 0	0000H			
Remap Capabilities	0K/8K		0K/1K/2K/4K	

T2-1.0 2057

2. The SFCF flash configuration SFR has different bit arrangements to control block mapping and visibility.

TABLE 2-2: BLOCK 1 REMAPPING AND VISIBILITY DIFFERENCES

SFCF[1:0]	SST89C5x	SSTx5xRDx
00	No Remap	8K Remap
01	1K Remap	0K Remap Block 1 is visible to the PC
10	2K Remap	0K Remap Block 1 is not visible to the PC
11	4K Remap	

T2-2.0 2057

3. The SFST flash status SFR has different levels of security assigned to the SB1, SB2 and SB3 bits. A double-clock status bit (EDC) was also added on the SST89x5xRDx.

TABLE 2-3: SECURITY SETTING DIFFERENCES

	SST89x5xRDx		SST89C5x	
SFST[7:5]	Block 1	Block 0	Block 1	Block 0
000	Unlock		Unlock	
001	Hard Lock	SoftLock	Hard Lock	SoftLock
010	SoftLock		SoftLock	
011	Hard Lock		Not Valid	
100	SoftLock		Hard Lock	
101	Hard Lock		Hard Lock	
110	Hard Lock	SoftLock	Hard Lock	
111	Hard Lock		Hard Lock	

T2-3.0 2057

4. The SST89x5xRDx does not support the Burst-Program IAP command. Replace it with equivalent Byte-Program commands.
5. There are differences in required values of SFDT and SFAH SFRs when performing the Prog-SBx and Prog-SCx commands. See Table 2-4.
6. There are differences in flash programming and erasure times. Proper use of flash-busy polling loops should eliminate compatibility issues. See Table 2-5

TABLE 2-4: IAP COMMAND SET DIFFERENCES

Operation	SFR Name	Command Value	
		SST89x5xRDx	SST89C5x
Prog-SB1	SFCM[6:0]	0FH	0FH
	SFDT[7:0]	AAH	55H
	SFAH[7:0]	X	80H
	SFAL[7:0]	X	X
Prog-SB2	SFCM[6:0]	03H	03H
	SFDT[7:0]	AAH	55H
	SFAH[7:0]	X	80H
	SFAL[7:0]	X	X
Prog-SB3	SFCM[6:0]	05H	05H
	SFDT[7:0]	AAH	55H
	SFAH[7:0]	X	80H
	SFAL[7:0]	X	X
Prog-SC0	SFCM[6:0]	09H	Not Valid
	SFDT[7:0]	AAH	
	SFAH[7:0]	5AH	
	SFAL[7:0]	X	
Prog-SC1	SFCM[6:0]	09H	Not Valid
	SFDT[7:0]	AAH	
	SFAH[7:0]	AAH	
	SFAL[7:0]	X	
Prog-RB0	SFCM[6:0]	Not Valid	08H
	SFDT[7:0]		55H
	SFAH[7:0]		80H
	SFAL[7:0]		X
Prog-RB1	SFCM[6:0]	Not Valid	09H
	SFDT[7:0]		55H
	SFAH[7:0]		80H
	SFAL[7:0]		X
Enable-Clock-Double	SFCM[6:0]	08H	Not Valid
	SFDT[7:0]	AAH	
	SFAH[7:0]	55H	
	SFAL[7:0]	X	

T2-4.0 2057

TABLE 2-5: PROGRAMMING AND ERASURE TIME DIFFERENCES

Parameter	SST89x5xRDx	SST89C5x
Chip-Erase Time	150ms (max)	11.7ms (max)
Block-Erase Time	100ms (max)	9.4ms (max)
Sector-Erase Time	30ms (max)	2.3ms (max)
Byte-Program Time	50µs (max)	110µs (max)

T2-5.0 2057

Application Note

3.0 EXTERNAL CODE AND DATA MEMORY

The following differences should be considered for the external code and data memory:

1. The SST89x5xRDx has 768 bytes of additional SRAM accessible as external data memory by default starting at address 0000H. Set the EXTRAM bit of the AUXR SFR to disable the additional SRAM and retain the behavior of the SST89C5x.
2. The SST89x5xRDx implements a disable-ALE bit in the AUXR SFR which will stop toggling of ALE when not accessing external code or data memory. No compatibility issues with the SST89C5x exist in default operation but this bit may be enabled to improve EMI characteristics.

Auxiliary Register (AUXR)

Location	7	6	5	4	3	2	1	0	Reset Value
8EH	-	-	-	-	-	-	EXTRAM	AO	xxxxxx00b

AO — Disable/Enable ALE
0: ALE is emitted at a constant rate of 1/3 the oscillator frequency in 6 clock mode and 1/6 f_{OSC} in 12 clock mode.
1: ALE is active only during a MOVX or MOVC instruction.

3. A second pair of DPTR registers overlay the standard set on the SST89x5xRD2. No compatibility issues with the SST89C5x exist but the second pair may be used to improve performance of block transfers or using DPTR in an interrupt routine. The visibility of the second pair is controlled by the DPS bit of the AUXR1 SFR.

Auxiliary Register 1 (AUXR1)

Location	7	6	5	4	3	2	1	0	Reset Value
A2H	-	-	-	-	GF2	0	-	DPS	xxxx00x0b

Symbol	Function
DPS	DPTR registers select bit. 0: DPTR0 is selected. 1: DPTR1 is selected.

4.0 WATCHDOG TIMER

The following differences should be considered for the watchdog timer:

1. The location of the WDTD SFR has moved from address 86H to 85H on the SST89x5xRDx.
2. The watchdog timer on the SST89x5xRDx operates off the system clock. The watchdog timer on the SST89C5x operates off a separate internal oscillator. Recompute the timer reload value based on external oscillator frequency and the equation stated in the data sheet. Note that the watchdog timer is not affected by the clock-doubler.

	SST89x5xRDx	SST89C5x
f_{WDT}	f_{OSC}	100Hz (typ) ~130Hz (max)

3. A WDOUT bit was added to the WDTC SFR to allow output of the watchdog reset signal. This bit should remain cleared to ensure compatibility with the SST89C5x.

Watchdog Timer Control Register (WDTC)

Location	7	6	5	4	3	2	1	0	Reset Value
C0H	-	-	-	WDOUT	WDRE	WDTS	WDT	SWDT	xxx00x00b

Symbol	Function
WDOUT	Watchdog output enable. 0: Watchdog reset will not be exported on Reset pin. 1: Watchdog reset if enabled by WDRE, will assert Reset pin for 32 clocks.

5.0 TIMER 2

The following differences should be considered for Timer 2:

1. The T2MOD SFR was added to the SST89x5xRDx and adds clock-out and down-counter functionality to Timer 2. Keep this SFR at the default value to insure compatibility with the SST89C5x.

Timer/Counter 2 Mode Control Register (T2MOD)

Location	7	6	5	4	3	2	1	0	Reset Value
C9H	-	-	-	-	-	-	T2OE	DCEN	00H

Symbol	Function
-	Not Implemented. Reserved for future use.
T2OE	Timer 2 Output Enable bit.
DCEN	Down Count Enable bit. When set, this allows Timer 2 to be configured as an up/down counter.

Application Note

6.0 INTERRUPTS

The following differences should be considered for interrupts:

1. Additional interrupt SFRs were added to support the PCA and brown-out modules. No compatibility issues should arise if these bits are not changed from the default.

Interrupt Enable (IE)

Location	7	6	5	4	3	2	1	0	Reset Value
A8H	EA	EC	ET2	ES	ET1	EX1	ET0	EX0	00H

Symbol	Function
EC	PCA Interrupt Enable.

Interrupt Enable A (IEA)

Location	7	6	5	4	3	2	1	0	Reset Value
E8H	-	-	-	-	EBO	-	-	-	xxxx0xxxb

Symbol	Function
EBO	Brown-out Interrupt Enable.

2. Additional interrupt SFRs (IPH and IPAH) were added allowing for a four-level interrupt priority scheme. No compatibility issues should arise if these bits are not changed from the default.

7.0 OTHER CHANGES

A significant number of additional SFRs were added to support the following features:

- Programmable Counter Array (PCA)
- Serial Peripheral Interface (SPI)
- Framing Error Detection (FED)
- Automatic Address Recognition (AAR)
- Port 4 (P4) for SST89x5xRD2 only

By default, these modules and two external interrupts in Port 4 are disabled so no compatibility issues are expected during code conversion.