SST89E/V516RDx and SST89E/V58RDx Memory Block Switching

Application Note
July 2008

1.0 INTRODUCTION

The SST89E/V516RDx and the SST89E/V58RDx are devices in the SST FlashFlex51 family of 8051 compatible microcontrollers. These microcontrollers contain two separate blocks of flash memory from which code may execute. One unique In-Application Programming (IAP) feature allows either of the flash memory blocks to be programmed while the other is simultaneously executing 8051 code.

Block switching is provided so that one block may service interrupts while the other is being programmed by remapping the interrupt vectors in the bottom 8K of program address space. The block switching feature is also the basis of the SST boot-strap loader (BSL), where Block 1 has the BSL code which can load user code into Block 0 from an external source and then block switch to execute the user code. This application note covers the usage of block switching feature found on the SST89E/V516RDx and the SST89E/V58RDx devices.

2.0 BLOCK SWITCH OPERATION

2.1 General Operation

The SC0 and SC1 configuration bits may be programmed using external host mode or IAP to determine the program memory organization of the MCU. When an external or power-on reset occurs, the SC0 and SC1 bits are logically inverted and become the default settings of the SFCF[1:0]. The SFCF[0] bit is alternatively known as the BSEL or block select bit and determines if Block 1 is mapped from 0000H to 1FFFH. Similarly, the SFCF[1] bit is known as the SWR or software reset bit and has two functions on the SST89E/V58RDx. First, on all devices, a 0 to 1 transition of the SWR bit will cause a software reset and the value of 1 will be preserved across the reset. Secondly, on the SST89E/V58RDx devices, the SWR bit determines if Block 1 is visible in the address range of E000H to FFFFH. Under a watchdog timer or brown-out reset, SWR will be preserved across the reset while BSEL will reflect the inverted value of SC0. Tables 2-2 and 2-1 summarize the values of SFCF[1:0] under different reset conditions.

TABLE 2-1: SFCF Reset Values (SST89E/V516RDx)

SC0	State of SFCF[1:0] after:		
	Power-on or External Reset	WDT Reset or Brown-out Reset	Software Reset
1	00	X0	10
0	01	X1	11

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TABLE 2-2: SFCF Reset Values (SST89E/V58RDx)

SC1	SC0	State of SFCF[1:0] after:		
		Power-on or External Reset	WDT or Brown-out Reset	Software Reset
1	1	00	X0	10
1	0	01	X1	11
0	1	10	10	10
0	0	11	11	11

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The primary concern when switching between flash memory blocks is to ensure that executions will continue at a valid instruction address after the switching occurs. This alignment between code in Block 0 and 1 may be difficult to achieve on variable instruction length architectures such as the 8051. The remainder of this document shows how the jump instructions and software reset can be used to perform the switching operation in a simple manner.

2.2 Switching off Block 1 on the SST89E/V516RDx

Figure 2-1 demonstrates different ways that Block 1 may be switched off on the SST89E/V54RD. If code is currently executing in Block 0, then as path (A) shows, simply set the BSEL bit to disable Block 1. After switching the block 1 off, the PC will end up at the same address in the new block plus the number of bytes of the instruction. The subsequent instruction (B) may optionally jump back to the portion of Block 0 that was hidden by Block 1. If code is executing in Block 1, then as path (C) shows, the software reset bit may be used to reset the PC back to 0000H after switching off Block 1 and then resume execution in Block 0.

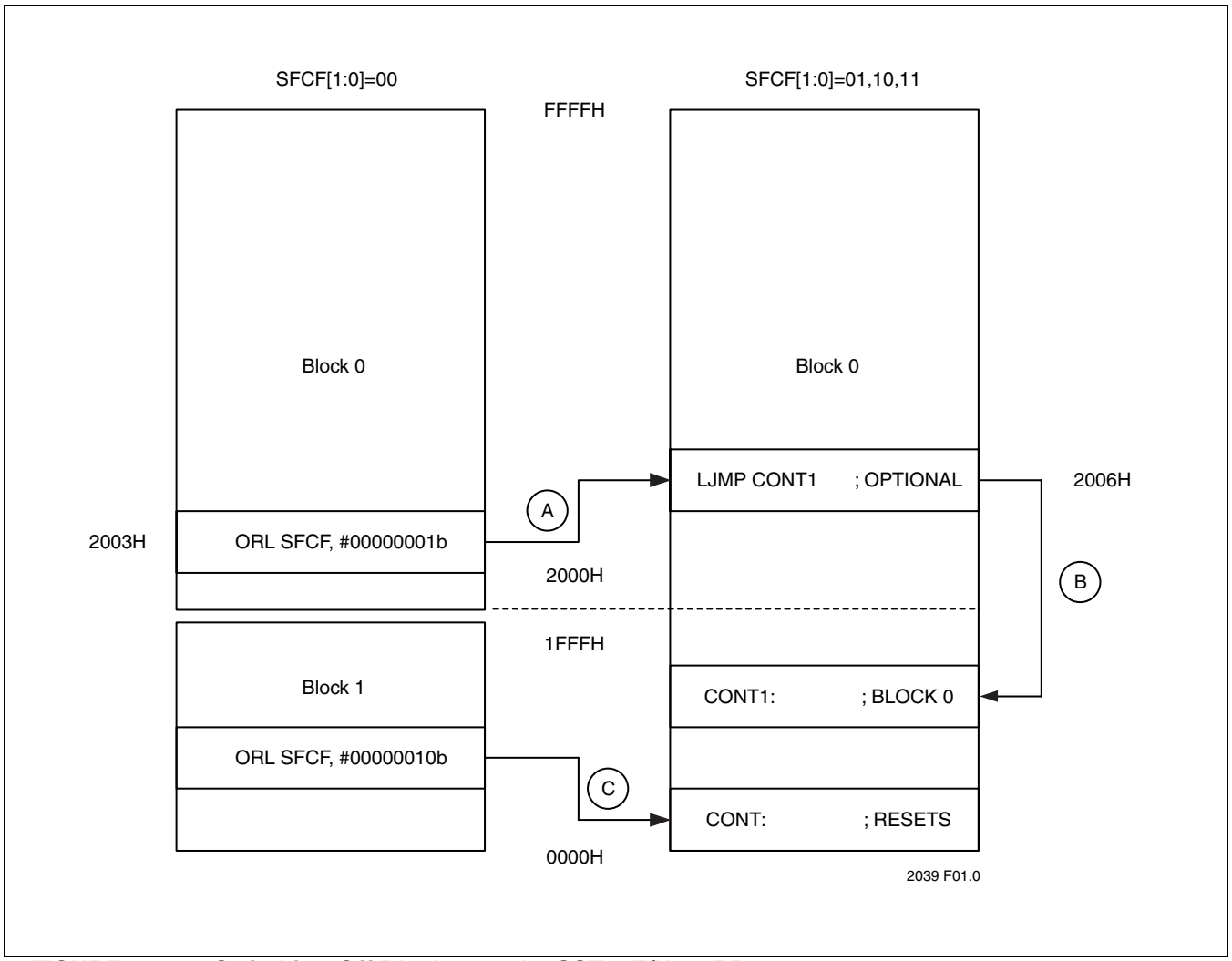

FIGURE 2-1: Switching Off Block 1 on the SST89E/V516RDx

2.3 Switching on Block 1 on the SST89E/V516RDx

Figure 2-2 demonstrates different ways that Block 1 may be switched on. To switch on Block 1, a jump instruction (A) must be used if code is executing below address 2000H to jump to an instruction above 2000H. Then the BSEL and SWR bits may be safely cleared to switch (B) Block 1 on. The subsequent instruction (C) may optionally jump back to Block 1 that is now visible.

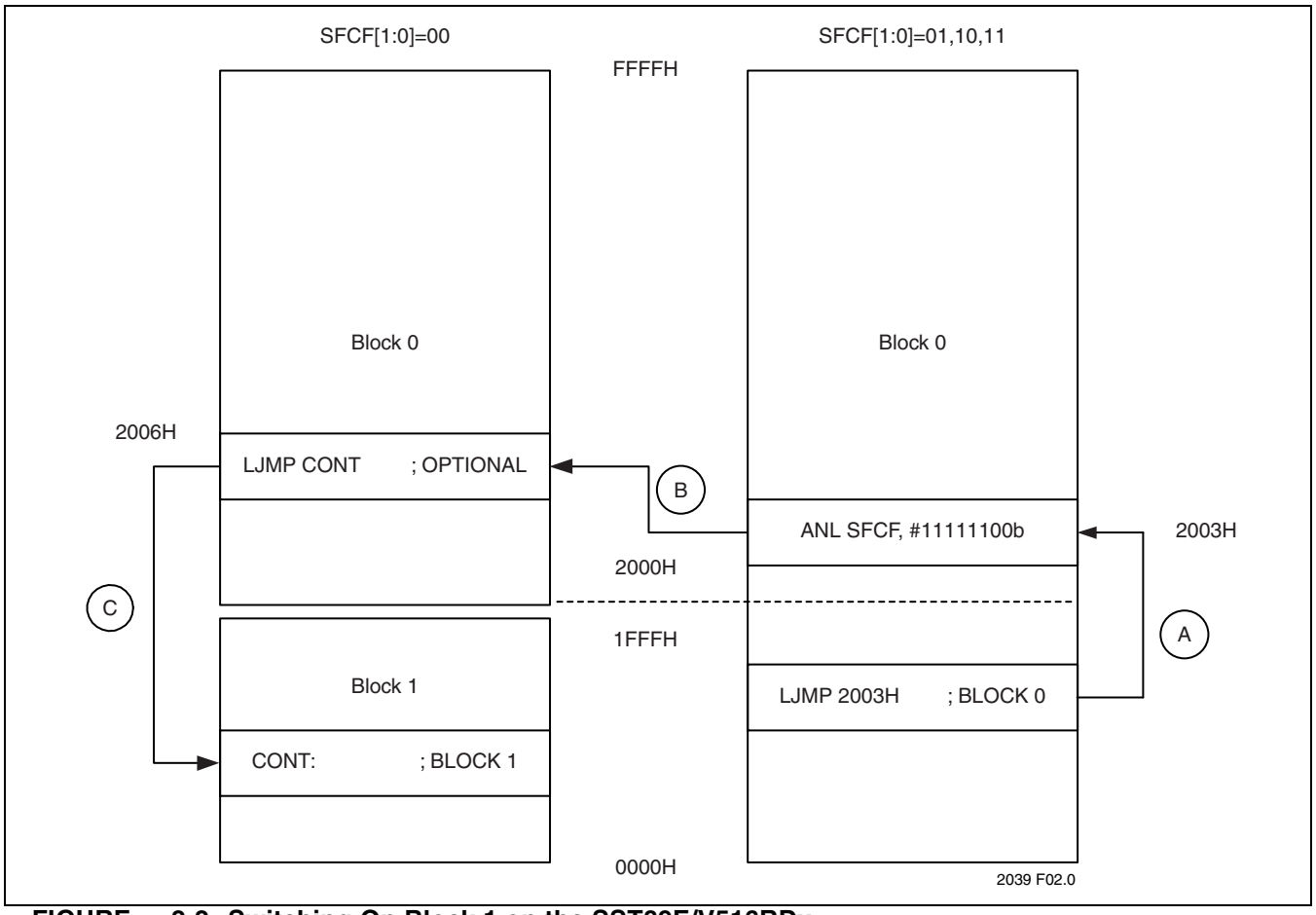

FIGURE 2-2: Switching On Block 1 on the SST89E/V516RDx

2.4 Switching off Block 1 on the SST89E/V58RDx

There are three ways to switch Block 1 off on the SST89E/V58RDx. If software reset is used, then as Figure 2-3 demonstrates, in all instances, the PC is reset to 0000H and execution resumes in Block 0. However, because SWR is set, this also means that Block 1 is not visible in the address range E000H to FFFFH.

Note that ORL SFCF, #00000010b and ORL SFCF, #00000011b are equivalent instructions, producing the same result.

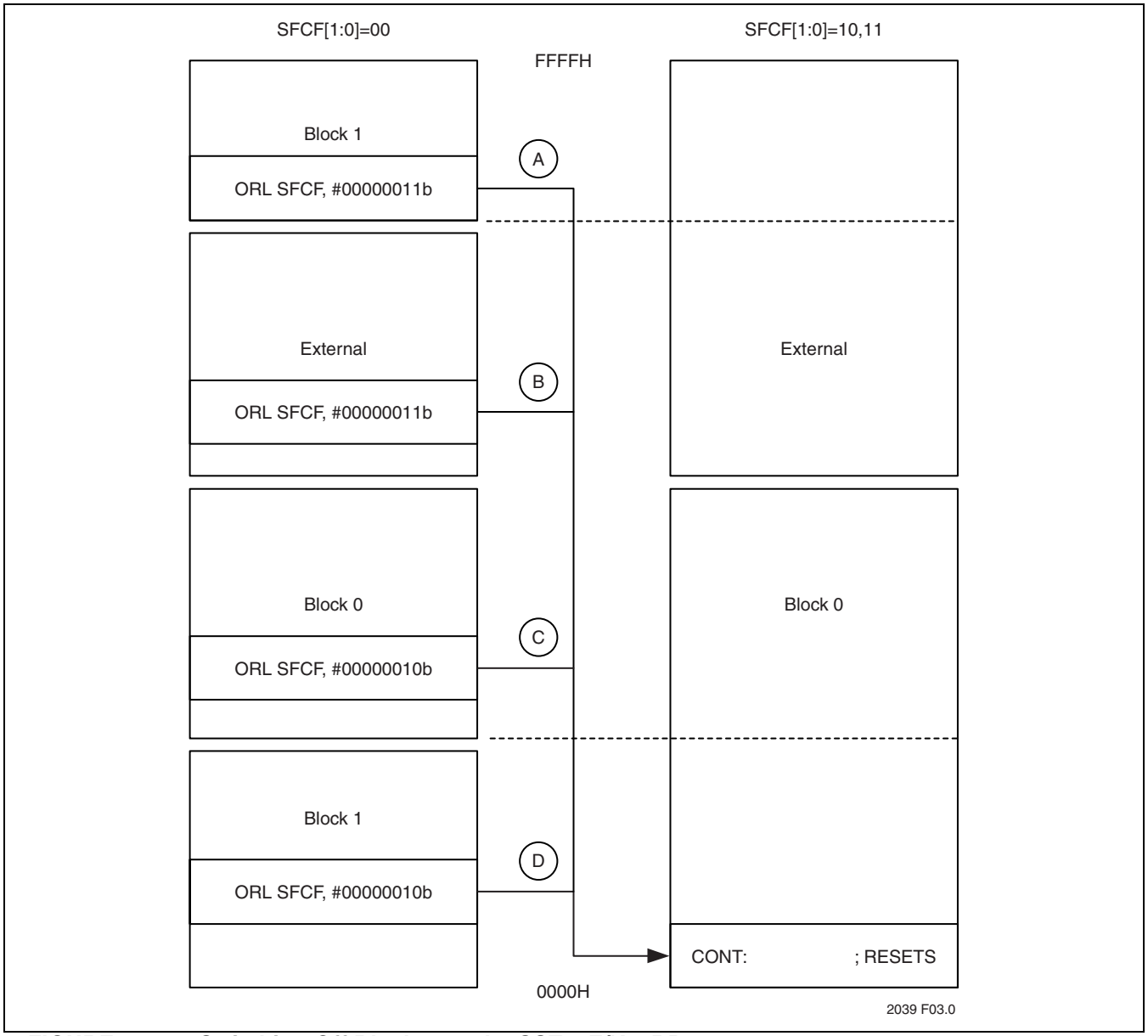

FIGURE 2-3: Switching Off Block 1 on the SST89E/V58RDx

If software reset is not used, then as Figure 2-4 demonstrates, a jump instruction (A) must be used to move the program counter above 2000H. Then the BSEL bit may be set to switch Block 1 overlay off. The subsequent instructions (E) may optionally jump back to Block 1 that is now visible.

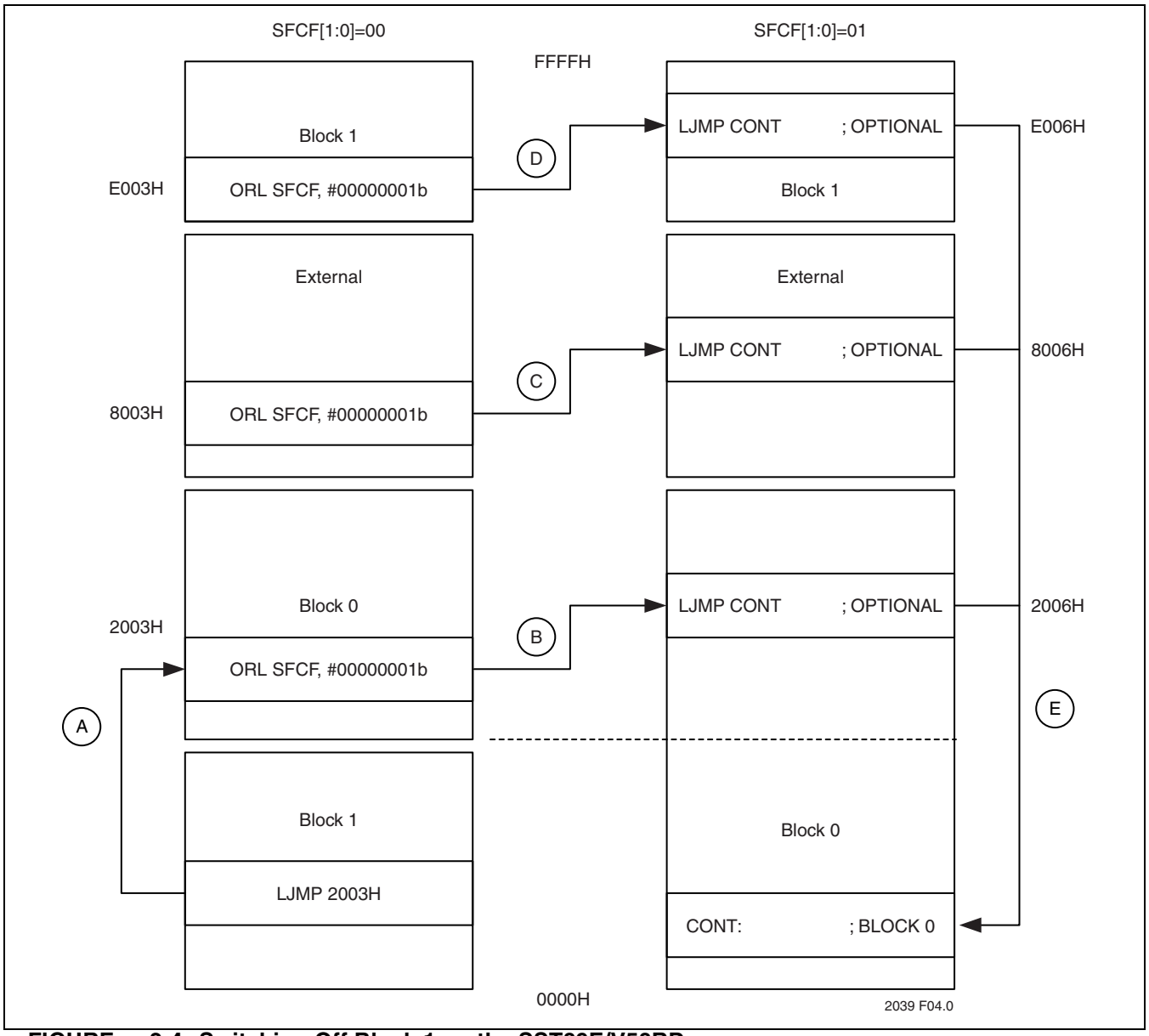

FIGURE 2-4: Switching Off Block 1 on the SST89E/V58RDx

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Because Block 1 is mapped to both the top and bottom address space of the SST89E/V58RDx devices, it is also possible to switch off Block 1 from the top address space as shown on Figure 2-5. Because the SWR bit is also set, in all instances, the PC is reset to 0000H and execution resumes in Block 0.

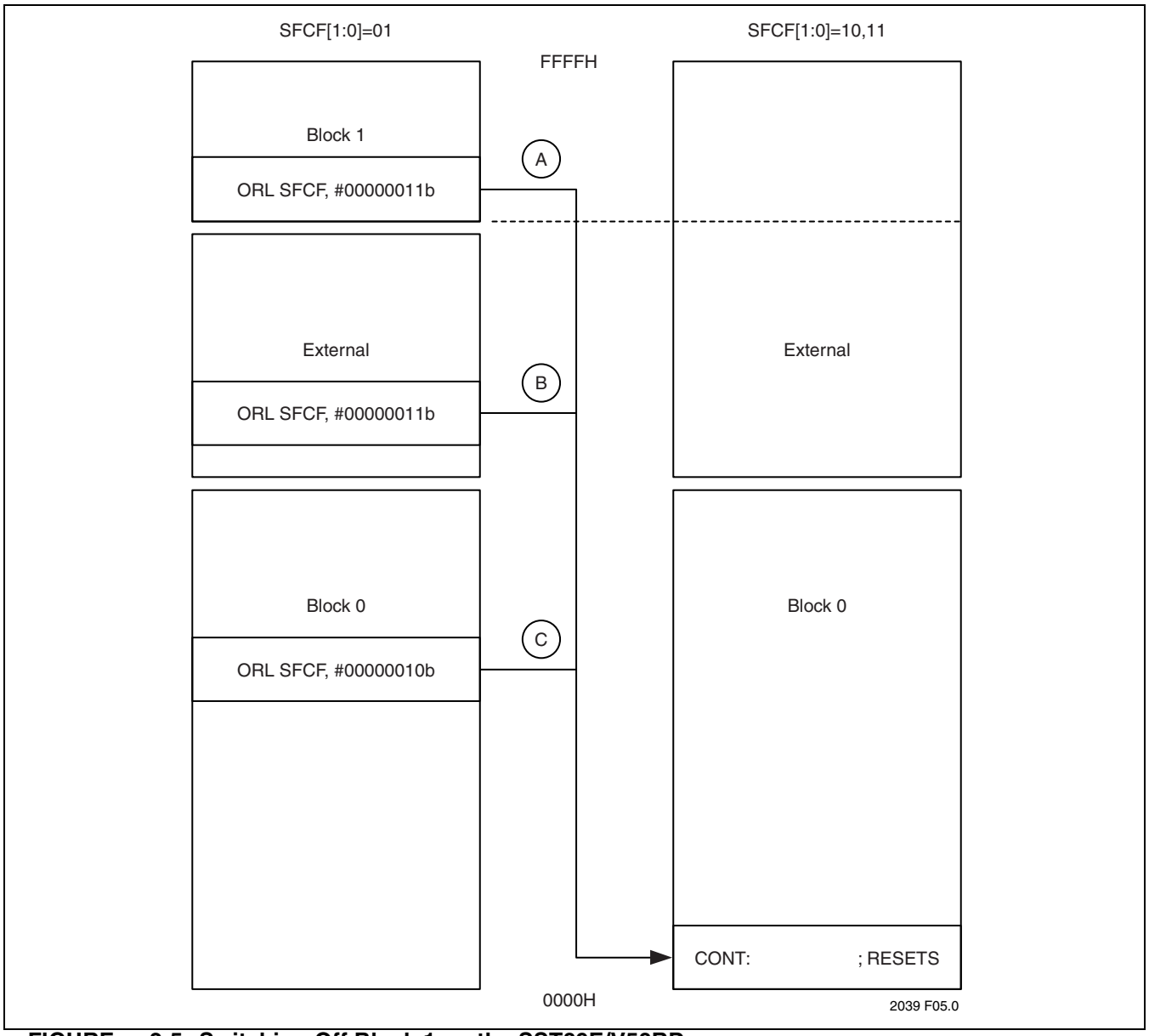

FIGURE 2-5: Switching Off Block 1 on the SST89E/V58RDx

2.5 Switching on Block 1 on the SST89E/V58RDx

Figure 2-6 demonstrates different ways that Block 1 may be switched on. To switch on Block 1, a jump instruction (A) must be used if code is executing below address 2000H to jump to an instruction address above 2000H. Then the BSEL and SWR bits may be safely cleared to switch (B) Block 1 on. The subsequent instruction (E) may optionally jump back to Block 1 that is now visible.

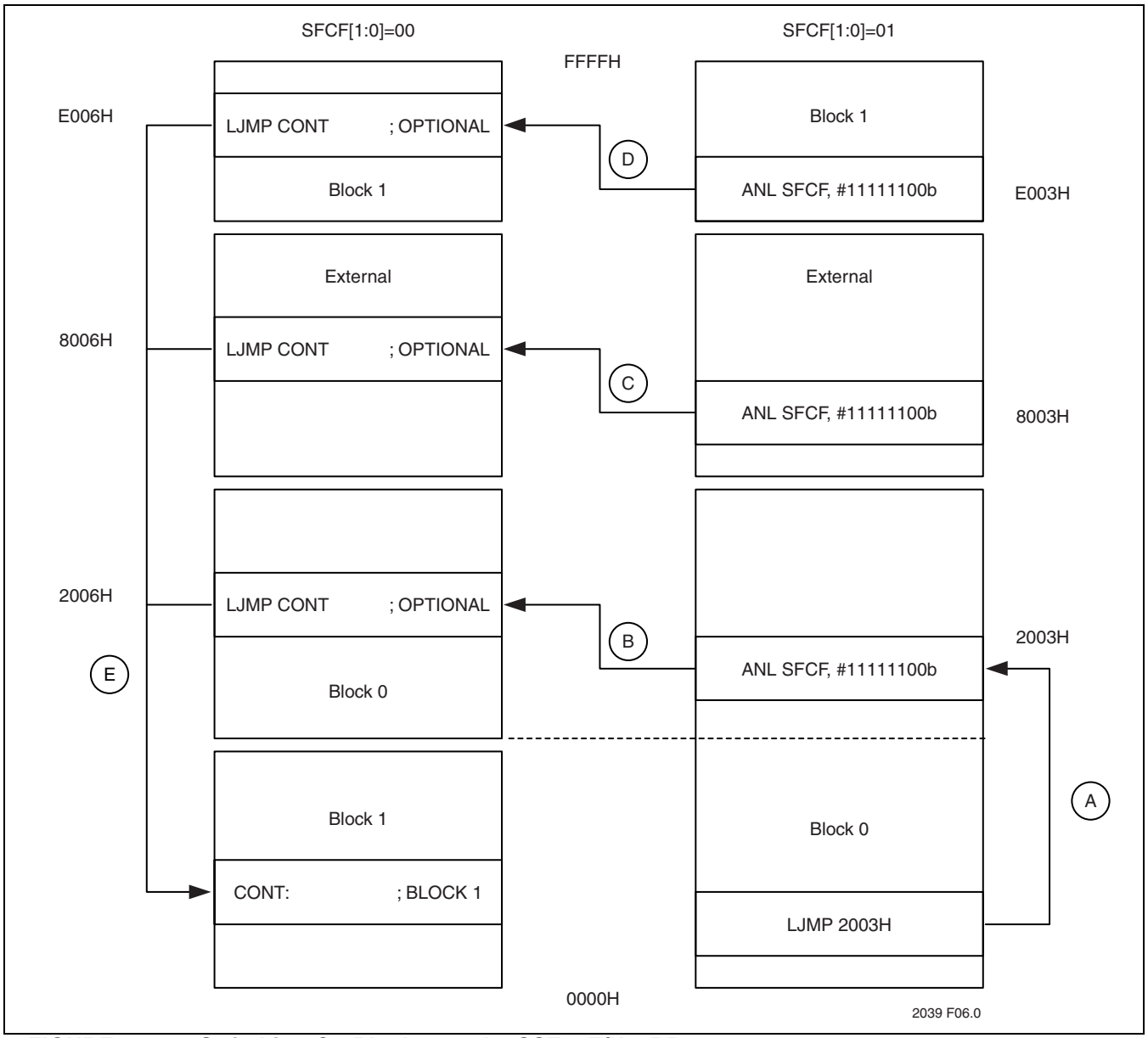

FIGURE 2-6: Switching On Block 1 on the SST89E/V58RDx

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3.0 BOOTSTRAP LOADER EXAMPLE

SST FlashFlex51 microcontrollers are pre-programmed with an example bootstrap loader in Block 1 demonstrating initial user program code loading and subsequent user code updating via the IAP operations. The BSL is made possible by the block-switching feature of the MCU. The BSL code is loaded into Block 1 with the SC0/SC1 bits unprogrammed so that Block 1 is mapped to the 0000H to 1FFFH address region. On startup, the BSL code checks the serial port for data. If no data is received within a preset time, the SWR and BSEL bits are used to initiate a block switch and software reset into Block 1 which contains user code. Otherwise, the BSL will parse the serial data based on a BSL command protocol allowing for reprogramming of Block via in-application programming.