Low-Power, High-Speed CMOS Analog Switches

Features

- 44-V Supply Max Rating
- ±15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 20 Ω
- Low Leakage—$I_{D(on)}$: 40 pA
- Fast Switching—t_{ON}: 100 ns
- Ultra Low Power Requirements—P_D: 0.35 µW
- TTL, CMOS Compatible
- Single Supply Capability

Benefits

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

Applications

- Audio and Video Switching
- Sample-and-Hold Circuits
- Battery Operation
- Test Equipment
- Hi-Rel Systems
- PBX, PABX

Description

The DG401/403/405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35 µW, typ) with high speed (t_{ON}: 100 ns, typ), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

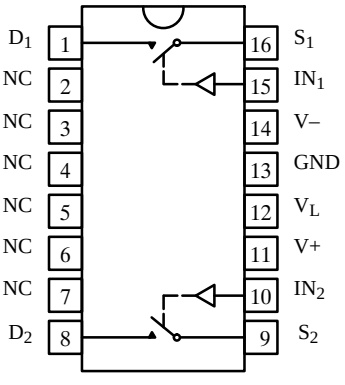
Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ±15-V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

Functional Block Diagrams and Pin Configurations

DG401

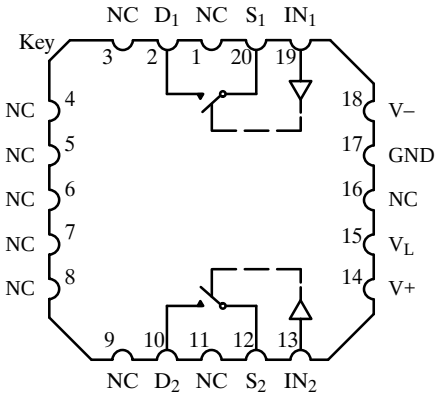
Dual-In-Line and SOIC



Top View

DG401

LCC



Top View

Two SPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

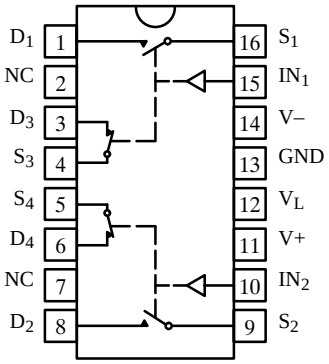
Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70049.

Functional Block Diagrams and Pin Configurations (Cont'd)

DG403

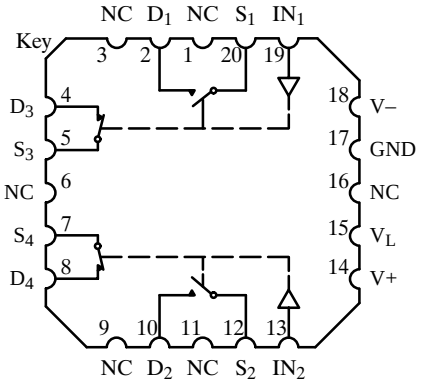
Dual-In-Line and SOIC



Top View

DG403

LCC



Top View

Two SPDT Switches per Package

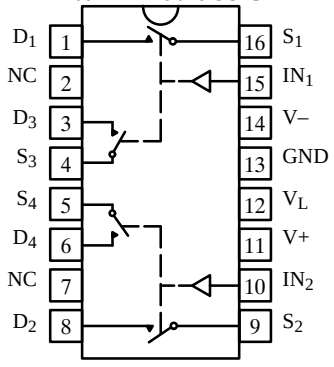
Truth Table

Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

DG405

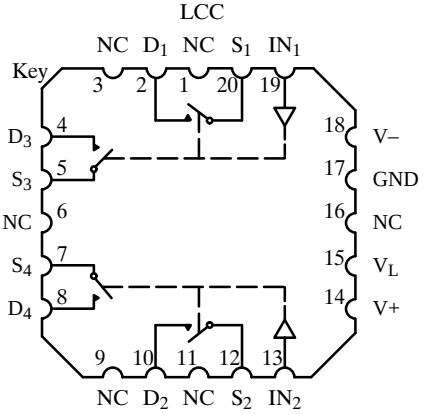
Dual-In-Line and SOIC



Top View

DG405

LCC



Top View

Two DPST Switches per Package

Truth Table

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Ordering Information

Temp Range	Package	Part Number
DG401		
–40 to 85°C	16-Pin Plastic DIP	DG401DJ
–55 to 125°C	16-Pin CerDIP	DG401AK
		DG401AK/883
	LCC-20	DG401AZ/883
DG403		
–40 to 85°C	16-Pin Plastic DIP	DG403DJ
	16-Pin Narrow SOIC	DG403DY
–55 to 125°C	16-Pin CerDIP	DG403AK
		DG403AK/883
	LCC-20	5962-8976301M2A
DG405		
–40 to 85°C	16-Pin Plastic DIP	DG405DJ
	16-Pin Narrow SOIC	DG405DY
–55 to 125°C	16-Pin CerDIP	DG405AK/883
	LCC-20	5962-89961012A

Absolute Maximum Ratings

V+ to V– . . . . . 44 V
GND to V– . . . . . 25 V
V_L . . . . . (GND – 0.3 V) to (V+) +0.3 V
Digital Inputs[a] V_S, V_D . . . . . (V–) –2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous . . . . . 30 mA
Current, S or D (Pulsed 1 ms 10% duty) . . . . . 100 mA
Storage Temperature (AK, AZ Suffix) . . . . . –65 to 150°C
(DJ, DY Suffix) . . . . . –65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] . . . . . 450 mW
16-Pin CerDIP[d] . . . . . 900 mW
16-Pin SOIC[e] . . . . . 600 mW
LCC-20[f] . . . . . 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C
e. Derate 7.6 mW/°C above 75°C
f. Derate 13 mW/°C above 75°C

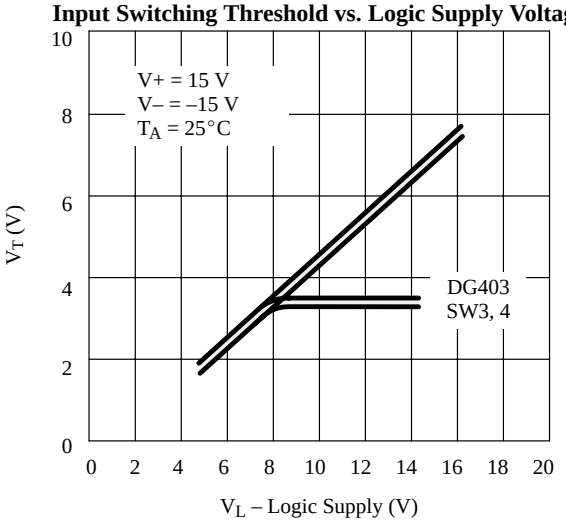
Specifications[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix –55 to 125°C Min[d]	A Suffix –55 to 125°C Max[d]	D Suffix –40 to 85°C Min[d]	D Suffix –40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		–15	15	–15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ±10 V V+ = 13.5 V, V– = –13.5 V	Room Full	20		35 45		45 55	Ω
Δ Drain-Source On-Resistance	$\Delta r_{DS(on)}$	I_S = –10 mA, V_D = ±5 V, 0 V V+ = 16.5 V, V– = –16.5 V	Room Full	3		3 5		3 5	Ω
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V– = –16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Hot	–0.01	–0.25 –20	0.25 20	–0.5 –5	0.5 5	nA
	$I_{D(off)}$		Room Hot	–0.01	–0.25 –20	0.25 20	–0.5 –5	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V– = –16.5 V V_S = V_D = ±15.5 V	Room Hot	–0.04	–0.4 –40	0.4 40	–1 –10	1 10	
Digital Control									
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V	Full	0.005	–1	1	–1	1	µA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	0.005	–1	1	–1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF See Figure 2	Room	100		150		150	ns
Turn-Off Time	t_{OFF}		Room	60		100		100	
Break-Before-Make Time Delay (DG403)	t_D	R_L = 300 Ω, C_L = 35 pF	Room	12	5		5		
Charge Injection	Q	C_L = 10,000 pF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60					pC
Off Isolation Reject Ratio	OIRR	R_L = 100 Ω, C_L = 5 pF f = 1 MHz	Room	72					dB
Channel-to-Channel Crosstalk	X_{TALK}		Room	90					
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room	12					pF
Drain Off Capacitance	$C_{D(off)}$		Room	12					
Channel On Capacitance	C_D, $C_{S(on)}$		Room	39					
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V– = –16.5 V V_{IN} = 0 or 5 V	Room Full	0.01		1 5		1 5	µA
Negative Supply Current	I–		Room Full	–0.01	–1 –5		–1 –5		
Logic Supply Current	I_L		Room Full	0.01		1 5		1 5	
Ground Current	I_{GND}		Room Full	–0.01	–1 –5		–1 –5		

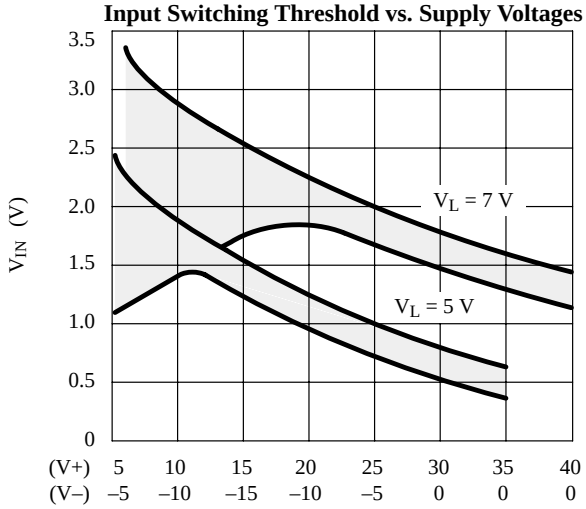
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

Typical Characteristics

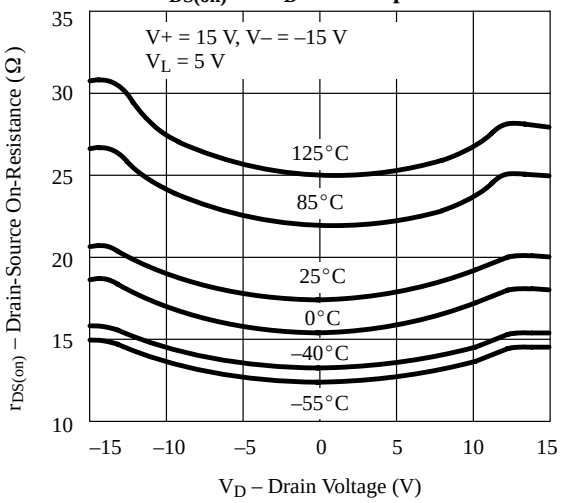
Input Switching Threshold vs. Logic Supply Voltage



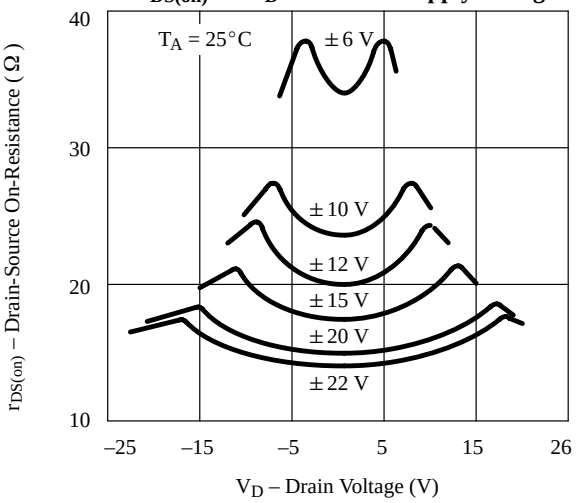
Input Switching Threshold vs. Supply Voltages



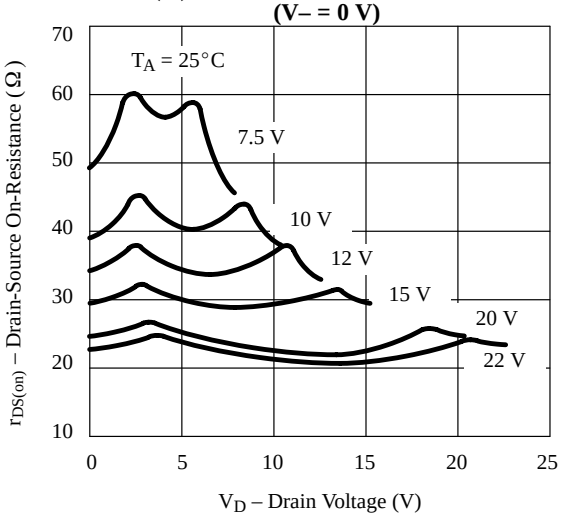
$r_{DS(on)}$ vs. V_D and Temperature



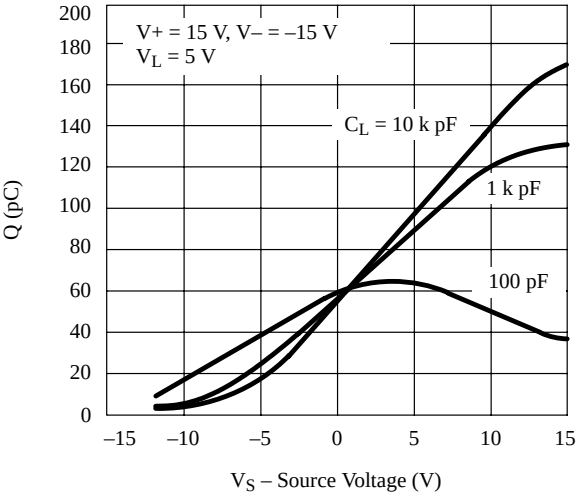
$r_{DS(on)}$ vs. V_D and Power Supply Voltage



$r_{DS(on)}$ vs. V_D and Power Supply Voltage (V– = 0 V)

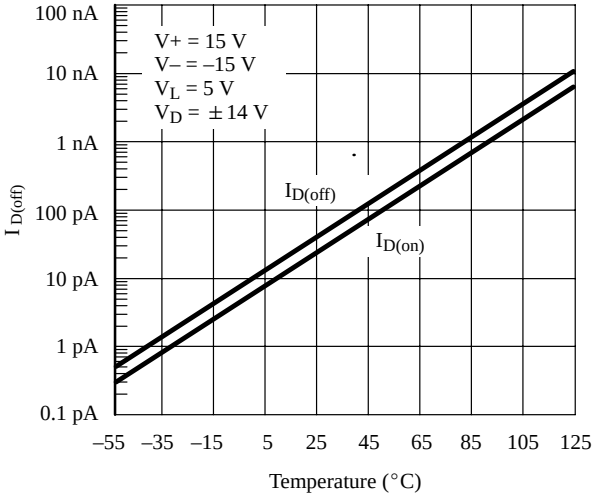


Charge Injection vs. Analog Voltage

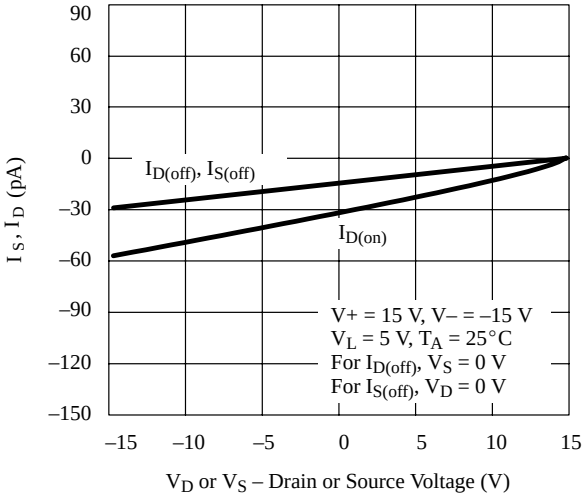


Typical Characteristics (Cont'd)

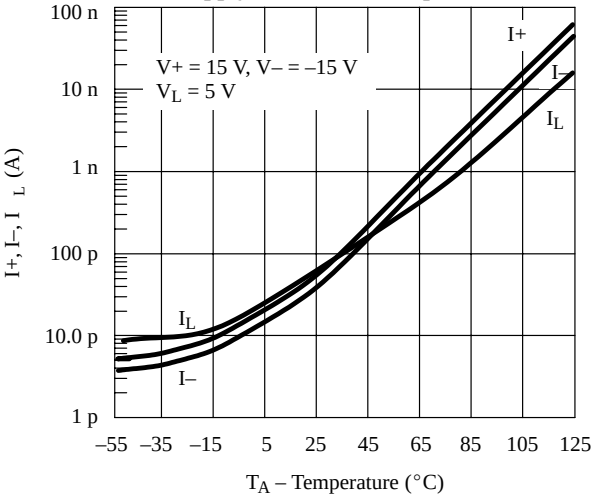
Leakage Current vs. Temperature



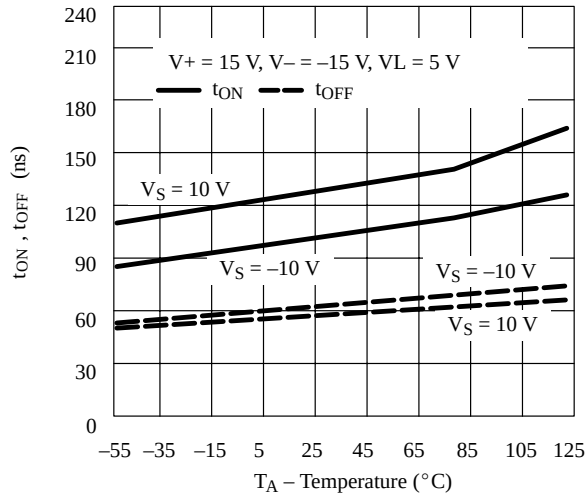
Leakage Current vs. Analog Voltage



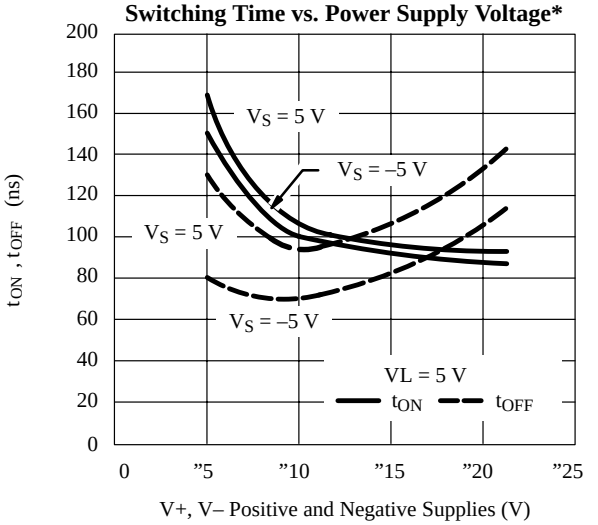
Supply Current vs. Temperature



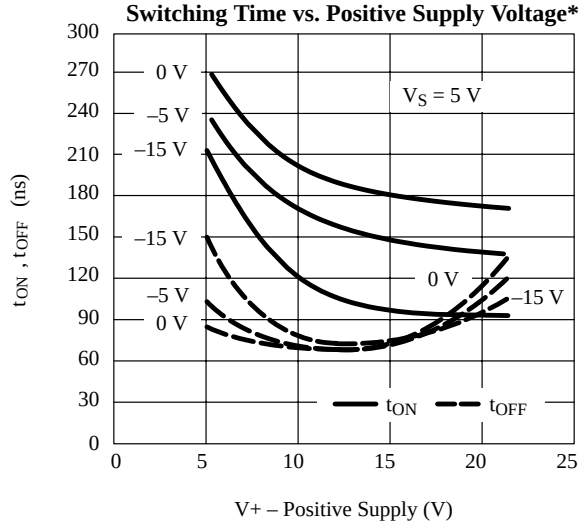
Switching Time vs. Temperature*



Switching Time vs. Power Supply Voltage*



Switching Time vs. Positive Supply Voltage*



*Refer to Figure 2 for test conditions.

Schematic Diagram (Typical Channel)

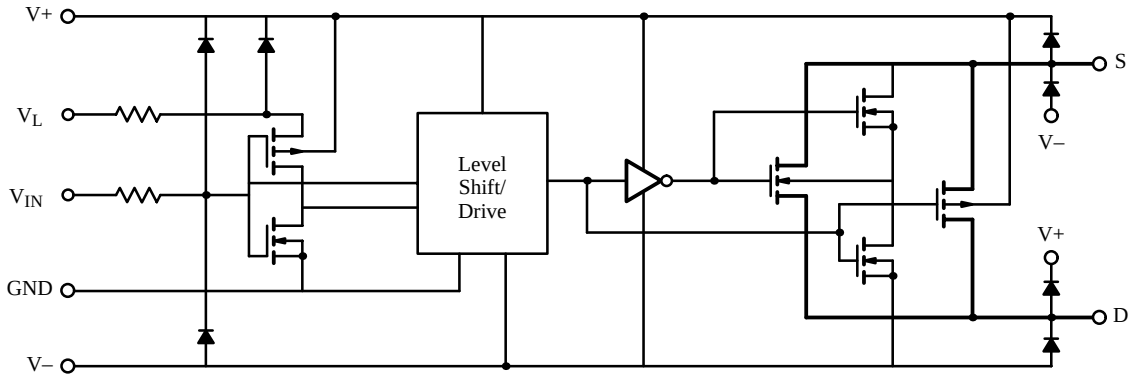
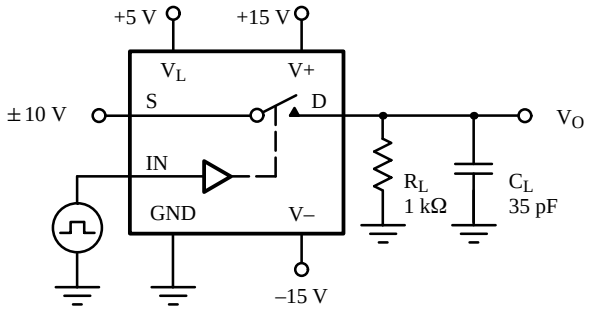


Figure 1.

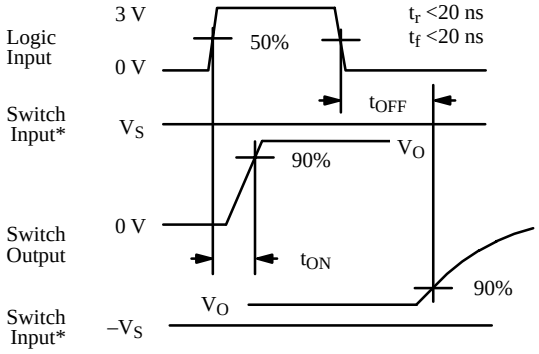
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



C_L (includes fixture and stray capacitance)

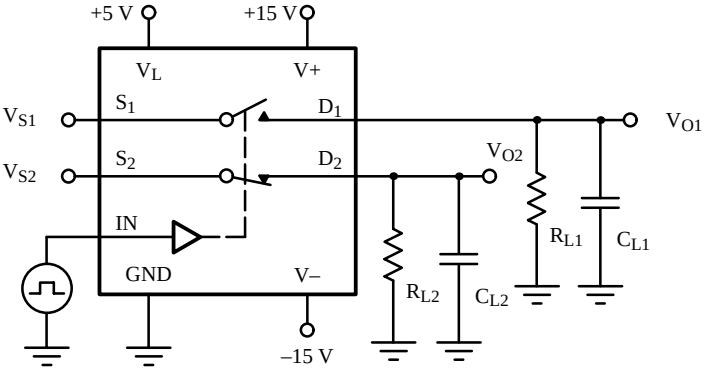
$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



*V_S = 10 V for t_{ON}, V_S = –10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time



C_L (includes fixture and stray capacitance)

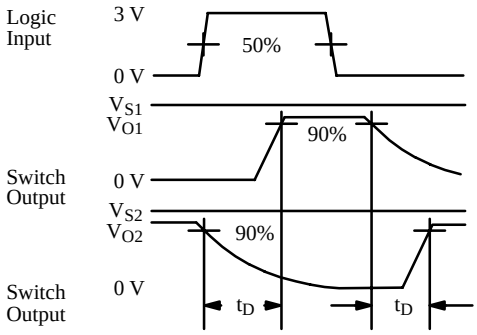
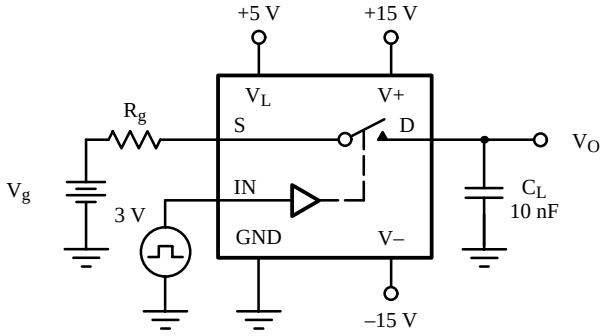


Figure 3. Break-Before-Make

Test Circuits (Cont'd)



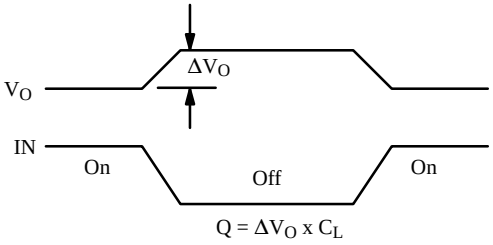


Figure 4. Charge Injection

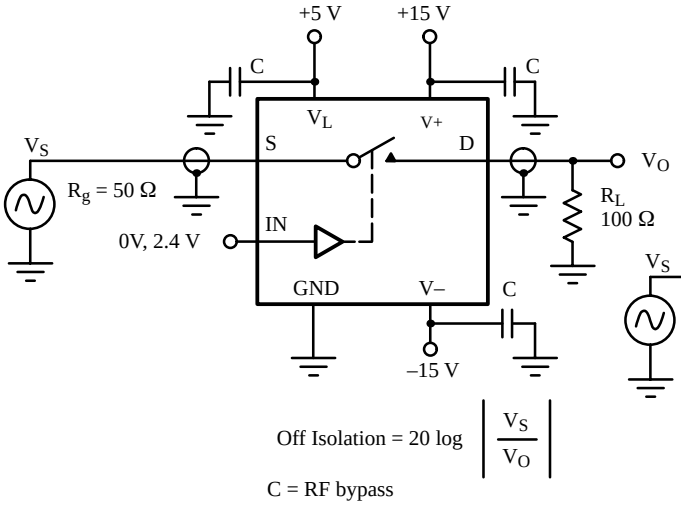


Figure 5. Off Isolation

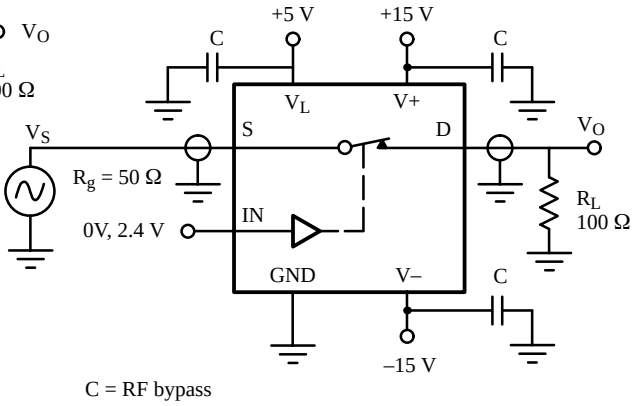


Figure 6. Insertion Loss

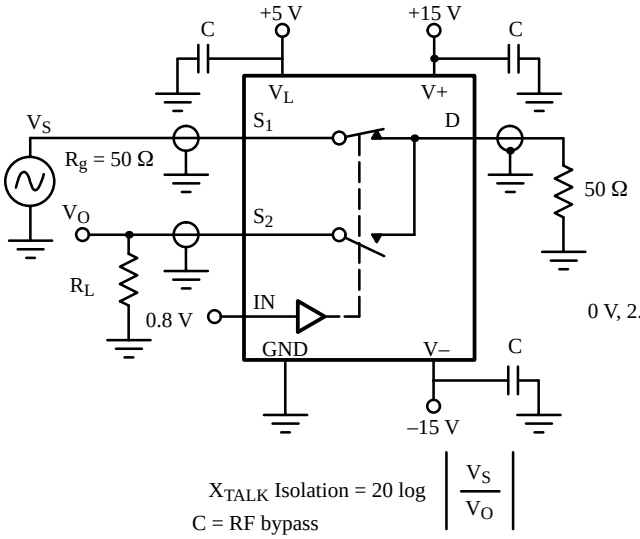


Figure 7. Crosstalk

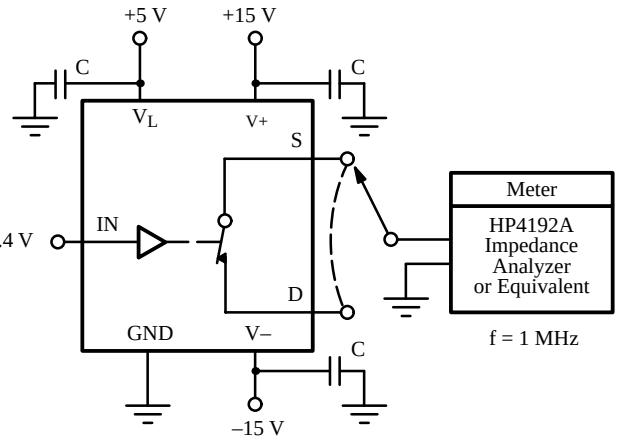


Figure 8. Capacitances

Applications

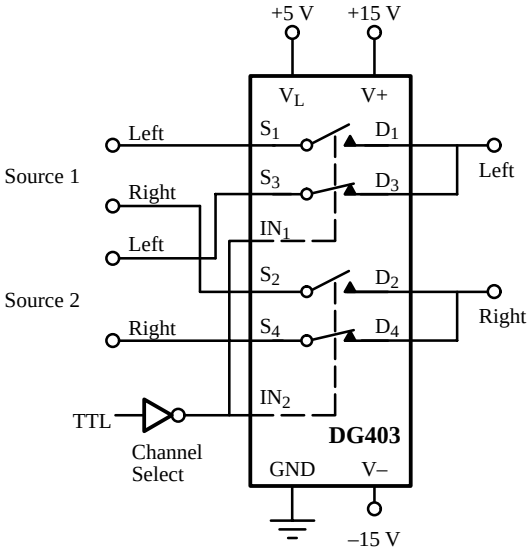


Figure 9. Stereo Source Selector

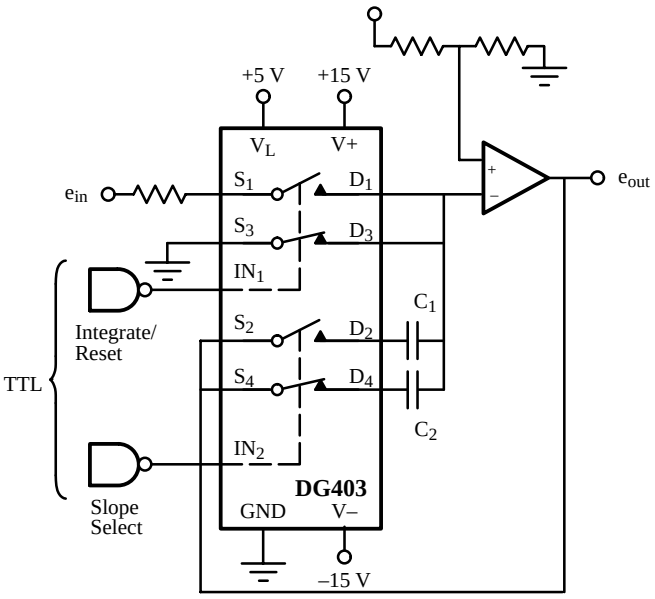


Figure 10. Dual Slope Integrator

Stereo Source Selector:

A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low on-resistance (<35 Ω) minimizes total harmonic distortion.

Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

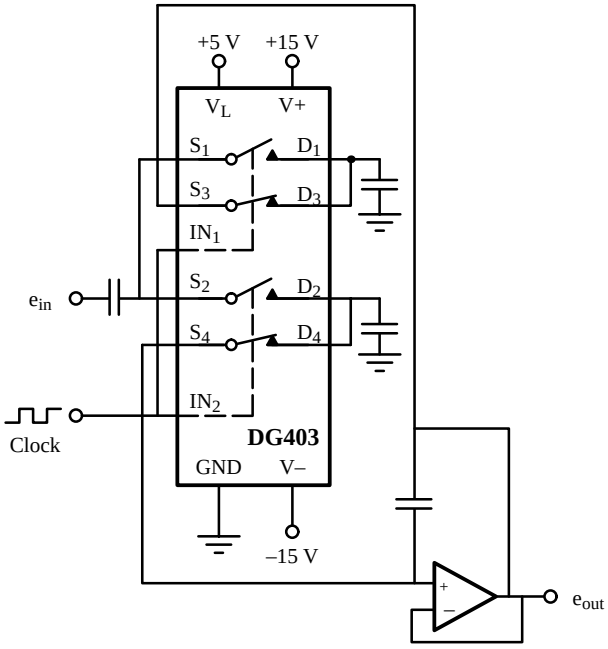


Figure 11. Band-Pass Switched Capacitor Filter

Applications (Cont'd)

Peak Detector:

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input e_{in}. If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{in} goes below e_{out} A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

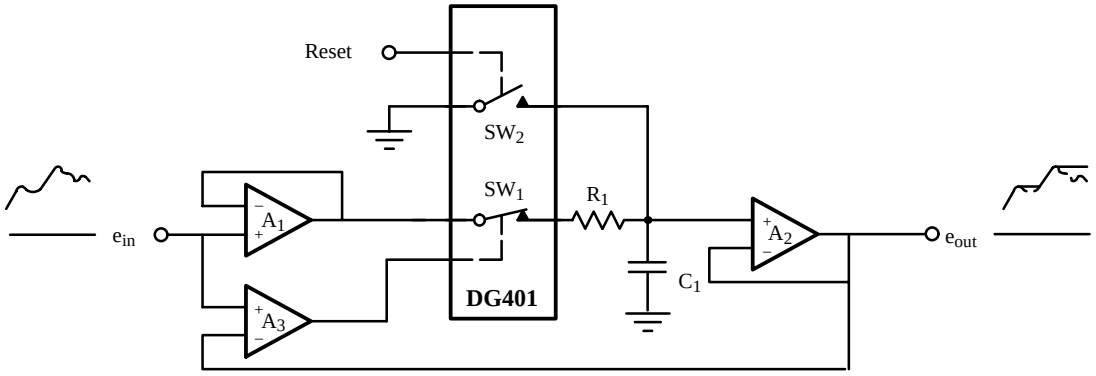


Figure 12. Positive Peak Detector